MT2533D Datasheet

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Document Revision History

Revision	Date	Description
0.1	15 August 2016	Initial draft
0.2	26 August 2016	Update power-on sequence, general operating conditions
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Features

Platform

- 208MHz ARM® Cortex®-M4 with FPU and MPU
- Fast wakeup of 7µs from sleep to active state
- Hardware DFS from 1.6MHz to 208MHz
- 17 DMA channels
- One RTC timer and six general purpose timers
- Crypto engine AES 128/192/256 bits
- True random number generator
- Ambient temperature from -40°C to 85°C

Memory

- 160kB SRAM
  - Zero-wait state
  - Maximum frequency 208MHz
- 32kB L1 cache
  - High hit rate
  - Zero-wait state
  - Maximum frequency 208MHz
- Embedded 32M bits flash
  - Sleep current 100nA
  - Maximum frequency 78MHz
- Embedded 32M bits pseudo SRAM
  - Sleep current 10µA
  - Maximum frequency 104MHz

Connectivity

- One USB2.0
- Two SDIO v2.0
- Three I2C (3.4Mbps)
- Three UART (3Mbps)
- Four SPI masters and one SPI slave (13MHz)
- I2S master or slave
- PCM master
- Dual PDM digital MIC
- Six PWM channels
- 38 GPIO
- 5 channel 12-bit AUXADC
- 3 x 3 matrix keypad

Bluetooth

- Bluetooth specification 4.2
- Dual mode (Bluetooth and Bluetooth LE)
- Integrated T/R switch, Balun and PA
- PA provides 7.5dBm output power
- -93dBm Bluetooth and -96.5dBm Bluetooth LE receiver sensitivity
- Up to 7 simultaneous active ACL links
- 1 simultaneous SCO or eSCO link with CVSD/mSBC coding

Audio codec

- AAC/SBC for Bluetooth audio
- CVSD/mSBC for Bluetooth speech
- PCM playback with 8-48kHz sample rate
- PCM record with 8kHz and 16kHz sample rate
- Dual mic noise suppression and acoustic echo cancellation
- Beamforming

Display

- Hardware 2D accelerator
  - 4-layer overlay
  - ARGB8888, RGB888, RGB565, ARGB6666
  - BitBlt supports 7 rotation types

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  - Alpha blending and font drawing
  - Hardware display rotation
- Supports four blending layers with individual color depth, window size, vertical and horizontal offset, source key, dither and alpha value.
- Read frame buffer format - RGB565, RGB888, ARGB8888, PARGB8888, ARGB6666, PARGB6666, YUYV422, index-4, index-2 and index-1 color.
- Supports DBI serial interface with resolution of 320 x 320 pixels and 30fps.
- Supports 1-lane MIPI DSI interface with resolution of 480x320 pixels and 30fps.

Package

- Highly integrated System in Package (SiP) technology
- MT2533D: 6.2mm × 5.8mm x 1.05mm 172-ball

  TFBGA with 0.4mm pitch

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Table of Contents

1. Overview 4

1.1. Platform 4
1.2. Multimedia 8
1.3. Audio 9
1.4. Bluetooth 9
1.5. Debugging 10
1.6. Package 10

2. Functional Overview 11

2.1. Host Processor Subsystem 11
2.2. Boot mode 13
2.3. Clock source architecture 14
2.4. Communication Interface 17
2.5. Peripherals 18
2.6. Analog baseband 19
2.7. Audio front-end 26

3. Bluetooth RF Subsystem 29

3.1. Bluetooth description 29
3.2. Functional specifications 30

4. Digital Signal Processing 34

4.1. Hardware features 34

5. Low Power Control System 35

5.1. MTCMOS power domain 35
5.2. Power modes 35
5.3. Power performance summary 36
5.4. Peripheral constraints and voltage for power mode 37

6. Pin Description 39

6.1. MT2533D Ball Diagram 39
6.2. MT2533D series pins 41
6.3. MT2533D pin multiplexing 49

7. System Configuration 55

7.1. System mode selection and trapping 55

8. Electrical Characteristics 56

8.1. Absolute maximum ratings 56
8.2. Operating conditions 56
8.3. Display controller 61
8.4. MIPI DBI TYPE-C interface characteristics 62
8.5. MIPI DBI TYPE-C Interface Color Coding 65
8.6. MIPI DSI interface characteristics 67
8.7. MIPI DSI interface color coding 71
8.8. Power On/Off sequence 71

9. Package Information 73

9.1. MT2533D mechanical data of the package 73
9.2. MT2533D thermal operating specifications 75
9.3. MT2533D lead-free packaging 75

10. Ordering Information 76

10.1. MT2533D top marking definition 76

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Lists of Tables and Figures

Table 1.1-1. MT2533D peripherals....7
Table 2.1-1. MT2533D series bus connection....13
Table 2.4-1. USB2.0 features....18
Table 2.6-1. Auxiliary ADC input channel....20
Table 2.6-2. Auxiliary ADC specifications....20
Table 2.6-3. Functional specifications of analog voice blocks....21
Table 2.6-4. Functional specifications of analog audio blocks....22
Table 2.6-5. MPLL specifications....24
Table 2.6-6. UPLL specifications....24
Table 2.6-7. DDS specifications....25
Table 2.6-8. HFOSC specifications....25
Table 2.6-9. LFOSC specifications....26
Table 2.7-1. Clock jitter of DAI and EDI....28
Table 3.2-1. Basic Data Rate – receiver specifications....30
Table 3.2-2. Basic Data Rate – transmitter specifications....30
Table 3.2-3. Enhanced Data Rate – receiver specifications....31
Table 3.2-4. Enhanced Data Rate – transmitter specifications....32
Table 3.2-5. Bluetooth LE – receiver specifications....32
Table 3.2-6. Bluetooth LE – transmitter specifications....33
Table 5.1-1. The MTCMOS power domain....35
Table 5.2-1. Power modes....35
Table 5.3-1. Current consumption in different power modes....36
Table 5.4-1. Always-on power domain peripherals....37
Table 5.4-2. INFRA_PD power-down domain peripherals....38
Table 6.1-1. MT2533D pin coordinates....39
Table 6.2-1. Acronym for pin types and I/O structure....41
Table 6.2-2. MT2533D digital pin function description and power domain....42
Table 6.2-3 MT2533D analog pin function description and power domain....47
Table 6.3-1. PinMux description....52
Table 7.1-1. Mode selection....55
Table 8.1-1. Absolute maximum ratings for power supply....56
Table 8.1-2. Absolute maximum ratings for I/O power supply....56
Table 8.1-3. Absolute maximum ratings for voltage input....56
Table 8.1-4. Absolute maximum ratings for storage temperature....56
Table 8.2-1. General operating conditions....56
Table 8.2-2. Recommended operating conditions for power supply....57
Table 8.2-3. Recommended operating conditions for voltage input....57
Table 8.2-4. Recommended operating conditions for operating temperature....57
Table 8.2-5. Electrical characteristics....57
Table 8.2-6. DCXO Characteristics (TA = 250C, VDD = 1.8V unless otherwise stated) (1)....59
Table 8.2-7. Functional specifications of XOSC32....60

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Table 8.2-8. Recommended parameters for 32.768kHz crystal oscillator 60
Table 8.2-9. ESD electrical characteristic of MT2533D 60
Table 8.4-1. Serial interface characteristics during write operation 63
Table 8.4-2. Serial interface characteristics during read operation 64
Table 8.6-1. HS clock transmission timing parameter 68
Table 8.6-2. HS data transmission timing parameter 69
Table 8.6-3. Low power mode timing parameter 70
Table 9.2-1. MT2533D thermal operating specifications 75
Table 10.1-1. Ordering information 76

Figure 1.1-1. MT2533D platform block diagram 5
Figure 1.1-2. MT2533D features 6
Figure 2.3-1. MT2533D clock source architecture 16
Figure 2.6-1. Block diagram of audio mixed-signal blocks 21
Figure 2.6-2. Block diagram of PLL clock sources 24
Figure 2.7-1. Digital circuits of the audio front-end 26
Figure 2.7-2. Timing diagram of Bluetooth application 27
Figure 2.7-3. Timing diagram of different clock rate Bluetooth applications 27
Figure 2.7-4. EDI Format 1: EIAJ (FMT = 0) 28
Figure 2.7-5. EDI Format 1: I2S (FMT = 1) 28
Figure 3.1-1. Bluetooth RF transceiver system 29
Figure 6.1-1. MT2533D ball diagram and top view 39
Figure 6.3-1. GPIO block diagram 49
Figure 8.4-1. 3-wire serial data interface 63
Figure 8.4-2. 4-wire serial data interface 63
Figure 8.4-3. 2-data pin mode 63
Figure 8.4-4. 3-wire serial interface 64
Figure 8.5-1. 3-wire serial interface (A0+8-bit) 65
Figure 8.5-2. 3-wire serial interface (A0+9-bit) 65
Figure 8.5-3. 4-wire serial interface write (8-bit) 66
Figure 8.5-4. 2-data-pin mode write (A0+8-bit) 66
Figure 8.5-5. 2-data-pin mode write (A0+9-bit) 67
Figure 8.5-6. 2-data-pin mode write (A0+12-bit) 67
Figure 8.6-1. HS clock transmission 68
Figure 8.6-2. HS data transmission in bursts 69
Figure 8.6-3. Turnaround procedure from MCU to display module 70
Figure 8.6-4. Turnaround procedure from display module to MCU 70
Figure 8.7-1. Pixel format of RGB565 71
Figure 8.7-2. Pixel format of loose RGB666 71
Figure 8.7-3. Pixel format of RGB565 71
Figure 8.8-1. Power on/off sequence 72
Figure 9.1-1 Outlines and dimensions of MT2533D TFBGA 6.2 mm*5.8 mm, 165-ball, 0.4 mm pitch package 75
Figure 10.1-1. Mass production top marking of MT2533D 76

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1. Overview

MediaTek MT2533D is a monolithic chip integrating leading edge analog baseband and radio circuitry based on the low-power CMOS digital design.

MT2533D is a feature-rich and powerful single-chip ready solution with Bluetooth or Bluetooth Low Energy (LE) connectivity support. Based on the ARM Cortex-M4 processor, MT2533D's processing power, along with high bandwidth architecture and dedicated hardware support, provides a platform for high-performance wearable and leading edge sensor control applications.

MT2533D is optimized for wearable products with the following strengths:

- Ultra small (6.2mm x 5.8mm) package size.
- Ultra low power consumption in active and idle modes, see section 5.3, "Power performance summary".
- Dynamic voltage scaling for optimized computing power.
- Built-in sensor hub and optimized sensor data capture engine.

1.1. Platform

MT2533D runs on Cortex-M4 RISC processor with the best trade-off between system performance and power consumption.

MT2533D also provides a co-processor to offload the control for Bluetooth. The microprocessor (Cortex-M4) is software programmable to enable the Bluetooth then focus its power to run the application.

For large amount of data transfers, high-performance direct memory access (DMA) with hardware flow control is used to enhance the data transaction speed while reducing the MCU processing load.

A special sensor DMA is also provided to support sensor data acquisition with low power consumption.

Targeted as a media-rich platform for wearable applications, MT2533D also provides hardware security digital rights management for copyright protection. To further safeguard and protect the manufacturer's investment in development, hardware flash content protection is provided to prevent unauthorized porting of the software load.

Figure 1.1-1 shows the detailed block diagram of MT2533D and Figure 1.1-2 shows the MT2533D features.

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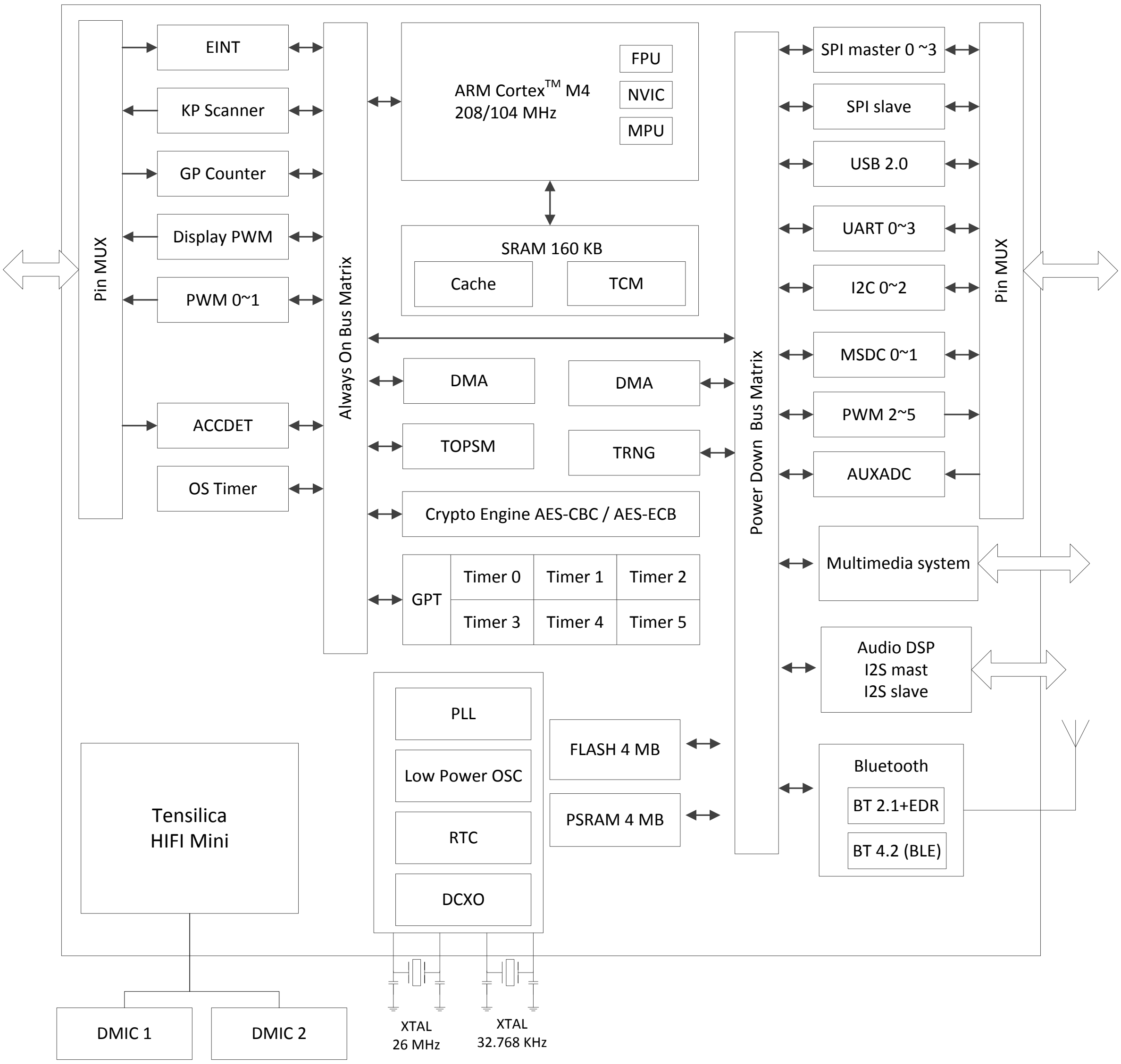

Figure 1.1-1. MT2533D platform block diagram

UART	**I2S**	**LCM**	**MIPI**
USB-HS	**SiP Flash 4MB**	**SiP SRAM 4MB**	**Keypad**
I2C	**Cortex-M4 with floating point unit 208MHz**		**ADC 12-bit**
SDIO	**SRAM/cache 160kB**	**DSP**	**Tensilica Hi-Fi Mini**
SPI	**RTC**	**Bluetooth® 2.1**	**Bluetooth® 4.2**

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- Co-processor offloads connectivity functionalities for Cortex-M4 with floating point unit
- Wi-Fi, NFC, Wireless Charging are optional by in-house standalone chips
- Supports internal 32.768kHz RTC

Figure 1.1-2. MT2533D features

1.1.1. MCU

The supported MCU has the following components and features.

- 208MHz ARM® Cortex®-M4 with floating point unit (FPU).
- High power efficiency with system DVFS.
  - 1.3V, 208MHz
  - 1.2V, 104MHz
  - 1.1V, 104MHz
  - 0.9V, 26MHz
  - 0.7V, 32.768kHz (RTC mode)
- Hardware DVS from deep sleep (0.7V) to active (0.9V or above)
- Fast wakeup of 7µs from sleep to active state
- Hardware DFS from 1.6MHz to 208MHz

1.1.2. Memory

MT2533D is embedded with MediaTek-patented low power PSRAM to improve active and idle current consumption.

- MT2533D supports serial flash with various operating frequencies and flash sizes.
  - 160kB SRAMs
  - Zero-wait state
  - Maximum frequency 208MHz
- 32kB L1 cache
  - High hit rate
  - Zero-wait state
  - Maximum frequency 208MHz
- SiP Embedded flash
  - Sleep current 100nA
  - Maximum frequency 78MHz
- SiP Embedded pseudo SRAM

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- Sleep current 10μA
- Maximum frequency 104MHz

1.1.3. Clock source

- 26MHz Digitally Controlled Crystal Oscillator (DCXO), that can supply reference clock for PLLs.
- USB PLL (UPLL) controlled by DCXO with 312MHz fixed frequency.
- Main PLL (MPLL) controlled by UPLL with a maximum frequency at 624MHz.
- Low Frequency RC oscillator (LFOSC) with a maximum frequency at 26MHz. Low power consumption with large frequency variation.
- High Frequency RC oscillator (HFOSC), with a maximum frequency at 312MHz. Low power consumption with large frequency variation.
- 32.768kHz low-speed external crystal (XOSC32K).
- 32.768kHz low-speed internal clock fed from DCXO (DCXO32K).
- 32.768kHz low-speed internal RC (EOSC32K) with large frequency variation (±5%).

1.1.4. Interfaces and peripherals

MT2533D supports UART, I2C, SPI, USB 2.0 HS/FS, SDIO and SD storage systems.

MT2533D brings together all necessary peripheral blocks for multimedia wearable products. The peripheral blocks include real-time clock, PWM and GPIOs, see Table 1.1-1.

Table 1.1-1. MT2533D peripherals

Peripheral	Counts	Description
Timer	3	–
Keypad	3 x 3 keypad scanner	With double key detection
PWM	6	–
UART	4	Up to 3Mbps
USB	1	2.0 High Speed
I2C	3	400kbps, up to 3.4Mbps
I2S	1 master 1 slave	–
SDIO	2	v2.0
SPI	4 masters 1 slave	–
LCM for display	1 serial I/F 1 lane MIPI DSI	MediaTek serial interface
ADC	5-channel 12-bit ADC	–
GPIO	38	Up to 38 ports with 20 interrupts
Crypto engine	1	• Supports AES-CBC/AES-ECB mode • Key length – 128/192/256 bits

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1.2. Multimedia

The MT2533D multimedia subsystem provides MediaTek proprietary serial interface and MIPI interface for LCM. The LCM resolution is up to 360 x 360 pixels.

The software-based codec can be used to process various video types. To take advantage of the high MCU performance, GIF and PNG decoders are implemented by the software.

In addition, MT2533D is implemented with a high-performance audio synthesis technology and a high-quality audio amplifier. MT2533D also provides voice command feature for wearable applications.

1.1.5. LCD controller

- Supports simultaneous connection to two serial LCD modules.
- Supports DBI serial interface.
- Supports MIPI DSI interface.
- Supported LCM formats — RGB565, RGB666, RGB888.
- Supports LCD module with maximum resolution of 320 x 320 pixels.
- Per pixel alpha channel.
- True color engine.
- Supports hardware display rotation.
- Capable of combining display memories with up to four blending layers.

1.1.6. MIPI DSI interface

- Single clock and data lanes.
- Throughput of up to 100Mbps.
- Bidirectional data transmission in low-power mode.
- Uni-directional data transmission in high-speed mode.
- 128-entry command queue for command transmission.
- Supports three types of video modes – sync-event, sync-pulse and burst mode.
- Supports non-continuous high-speed transmission in data lanes.
- Supports command mode frame transmission free run.
- Supports peripheral tearing effect (TE) and external TE signal detection.
- Supports low power mode control.
- Supports low frame-rate (LFR) technique.

1.1.7. 2D accelerator

- Supports 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565 and 24-bpp ARGB6666.
- 4 layers of overlay with individual color format, window size, source key, constant alpha and rotation.
- Rectangle fill with constant.
- Bit-boundary block transfer (BitBlt). Supports up to seven rotation types.

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- Alpha blending with seven rotation types, per-pixel alpha and pre-multiplied alpha.
- Font drawing. Normal font and anti-aliasing font (Display Adaptive Ambient Light Controller).

1.1.8. Display adaptive ambient light controller

- 33-bin weighted histogram.
- DRE enhancement for sunlight visibility.
- CABC compensation for backlight power saving.

1.3. Audio

Using a highly integrated mixed-signal audio front-end, the MT2533D architecture enables audio interfacing with direct connection to the audio transducers. The audio interface integrates A/D converters for voice band, as well as high-resolution stereo D/A converters for both audio and voice bands.

1.1.9. Audio CODEC

- Supports AAC and SBC codec decoding for Bluetooth audio.
- Supports CVSD and mSBC codec for Bluetooth speech.
- Pure PCM playback for 8-48kHz sample rate.
- Pure PCM record for 8kHz and 16kHz sample rates.

1.1.10. Audio interface and audio front-end

- Pure PCM record for 8kHz and 16kHz sample rates.
- Supports master I2S interface.
- Supports master PCM interface.
- Supports Dual PDM MIC.
- High-resolution D/A converters for stereo audio playback.
- Voice band A/D converter support.
- Stereo to mono conversion.

1.4. Bluetooth

MT2533D offers a highly integrated Bluetooth radio and baseband processor. Only a minimum of external components is required.

MT2533D is fully compliant with Bluetooth version 4.2, upgradable to later versions, including BR/EDR and Bluetooth LE and offers enhanced data rates of up to 3Mbps. It also provides the coexistence protocol with IEEE 802.11 protocol.

1.1.11. Radio

- Fully compliant with Bluetooth core specification 4.2.
- Low-IF architecture with high degree of linearity and high order channel filter.
- Integrated T/R switch and balun.

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- Fully integrated PA provides 7.5dBm output power.
- -95dBm sensitivity with interference rejection performance.
- Hardware AGC dynamically adjusts receiver performance in changing environments.

1.1.12. Baseband

- Up to seven simultaneous active ACL links.
- Up to eight simultaneous active Bluetooth LE links.
- A single SCO or eSCO link with CVSD/mSBC coding.
- Up to two simultaneous ACL slave links and four simultaneous Bluetooth LE links for audio or voice application, basic rate A2DP.
- AFH and PTA collaborative support for WLAN/Bluetooth coexistence.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission.
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption.
- Channel quality driven data rate adaptation.
- Channel assessment for AFH.

1.1.13. Core

- Feasibility Bluetooth host subsystem in Cortex-M4 to support customized applications.
- Embedded processor for Bluetooth controller subsystem with built-in memory system.
- Fully verified ROM based system with code patch for feature enhancement.

1.5. Debugging

The JTAG interface enables in-circuit debugging of the software program with the CPU. With this standardized debugging interface, MT2533D provides developers with a wide range of options in choosing ARM development kits from different third party vendors.

1.6. Package

The MT2533D device is offered in a 6.2mm × 5.8mm, 172-ball, 0.4mm pitch, TFBGA package.

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2. Functional Overview

2.1. Host Processor Subsystem

2.1.1. ARM® Cortex®-M4 with FPU

The Cortex-M4 with FPU is a low-power processor with 3-stage pipeline Harvard architecture. It has reduced pin count and low power consumption and delivers high performance efficiency and low interrupt latency, making it ideal for embedded microcontroller products.

The processor incorporates:

- IEEE754-compliant single-precision floating-point computation unit (FPU).
- A Nested Vectored Interrupt Controller (NVIC) to achieve low latency interrupt processing.
- Enhanced system debugging with extensive breakpoint and trace capabilities.
- An optional Memory Protection Unit (MPU) to ensure platform security robustness.

The Cortex-M4 executes the Thumb®-2 instruction set with 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers. The instruction set is fully backward compatible with Cortex-M3/M0+.

MT2533D has further enhanced the Cortex-M4 processor to reduce the power by another 11% (in Dhrystone) compared to the original Cortex-M4, a significant low power achievement for IoT and wearable applications.

2.1.2. Cache controller

A configurable 32kB cache is implemented to improve the code fetch performance when CPU accesses a non-zero wait-state memory such as EMI, external flash or boot ROM through the on-chip bus.

The core cache is a small block of memory containing a copy of small portion of cacheable data in the external memory. If CPU reads a cacheable datum, the datum will be copied to the core cache. Once the CPU requests the same datum again, it can be obtained directly from the core cache (called cache hit) instead of fetching it again from the external memory to achieve zero wait-state latency.

The cache can be disabled and this block of memory can be turned into tightly coupled memory (TCM), a high-speed memory for normal data storage. The sizes of TCM and cache can be set to one of the following four configurations:

- 32kB cache, 128kB TCM
- 16kB cache, 144kB TCM
- 8kB cache, 152kB TCM
- 0kB cache, 160kB TCM

2.1.3. Memory management

Three types of memories are implemented for use:

1) On-die memories (SRAMs) with up to 160kB at CPU clock speed with zero wait state.
2) Embedded flash of 32Mbits to store programs and data.

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3) Embedded pseudo SRAM (PSRAM) of 32Mbits for application storage.

160kB SRAMs are composed of TCMs and L1 caches. L1 cache (up to 32kB) is implemented to improve processor access performance of the long latency memories (flash and PSRAM).

TCMs are designed for high speed, low latency and low power demanding applications. Each TCM has its own power state; active, retention or power-down. TCM must be in active state for normal read and write access. Retention state saves the SRAM content and consumes the minimum leakage current with no access. Power-down loses the content and consumes almost zero power.

Other internal AHB masters, such as DMA or multimedia sub-system, can also access TCMs for low power applications. These applications can run on TCM without powering on the PSRAM or flash, to save more power.

Boot ROM is also implemented for processor boot–up and its content is unchangeable.

2.1.4. Memory Protection Unit

The Memory Protection Unit (MPU) is an optional component to manage the CPU access to memory. The MPU provides full support for:

- Protection regions (up to 8 regions and can be further divided up into 8 sub-regions).
- Overlapping protection regions, with region priority.
- Access permissions.
- Exporting memory attributes to the system.

The MPU is useful for applications where a critical code has to be protected against the misbehavior of other tasks. It can be used to define access rules, enforce privilege rules and separate processes.

2.1.5. Nested Vectored Interrupt Controller

The Nested Vectored Interrupt Controller (NVIC) supports up to 64 maskable interrupts and 16 interrupt lines of Cortex-M4 with 64 priority levels. The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked or nested interrupts to enable tail-chaining of interrupts. The processor supports both level and pulse interrupts with programmable active-high or low control.

2.1.6. External Interrupt Controller

The external interrupt or event controller (EINT) consists of 32 edge/level detector lines used to generate interrupt or event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both and level) and can be masked independently. A pending register maintains the status of the interrupt requests. Up to 31 GPIOs can be connected to 20 external interrupt lines.

2.1.7. Bus architecture

To better support various IoT applications, MT2533D adopts 32-bit multi-AHB matrix to provide low-power, fast and flexible data operation. Table 2.1-1 shows the interconnections between bus masters and slaves.

- The bus masters include Cortex-M4, four SPI masters, SPI slave, debug system, Multimedia (MM) system, USB and three DMAs.
- The bus slaves include the Always On (AO) domain APB peripherals, Power Down (PD) domain APB peripherals, TCM, SFC, EMI, MDSYS and BTSYS.

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Table 2.1-1. MT2533D series bus connection

Master / Slave	ARM Cortex-M4	AO DMA	PD DMA	Sensor DMA	USB	MM SYS	Debug SYS	SPI Master	SPI Slave
AO APB Peripherals	●	●							
PD APB Peripherals	●		●	●				●	●
TCM	●	●	●	●		●		●	●
EMI	●	●	●	●	●	●	●	●	●
SFC	●	●	●	●				●	●
Audio DSP	●		●	●				●	●
BTSYS	●		●	●				●	●

2.1.8. Direct Memory Access Controller

MT2533D chipset features three Direct Memory Access (DMA) controllers, containing a total of 17 channels in power-down and always-on power domains, respectively. They manage data transfer between the peripheral devices and memory.

There are three types of DMA channels in the DMA controller – full-size DMA channel, half-size DMA channel and virtual FIFO DMA for different peripheral devices. DMA controllers support ring-buffer and double-buffer memory data transactions, which makes the memory control easier.

To improve bus efficiency, the DMA controllers provide an unaligned-word access function. When this function is enabled, it can automatically convert the address format from the unaligned type to aligned type, ensuring compliance with the AHB/APB protocol.

Each peripheral device is connected to a dedicated DMA channel that can configure transfer data sizes, source address and destination address by software. The DMA controllers can be used with the following peripherals:

- Two MSDCs
- Two I2Cs
- Four UARTs
- A single BTIF

2.2. Boot mode

While the chip is starting up, the on-chip boot ROM is executed to determine the next booting sequence, either flash download mode or normal boot mode.

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- Flash download mode. The bootloader is located in the embedded flash and can be reprogrammed through UART or USB interface. For USB, there are two methods to trigger the download flow – USB auto-detection by USB plug-in or pulling the pin GPIO_B2 to low.
- Normal boot up mode. In this mode, the boot ROM copies the bootloader from embedded flash to the internal memory, without entering flash download mode. When the system finishes boot ROM execution, it will jump to bootloader and execute it.

2.3. Clock source architecture

The clock controller (see Figure 2.3-1) distributes the clocks from different oscillators to the core circuit and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness. The clock controller features:

- **Clock prescaler** — to get the best trade-off between speed and current consumption. The clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- **Safe clock switching** — clock sources can be changed safely on the fly through a configuration register.
- **Clock management** — to reduce the power consumption, the clock controller can stop the clock of the core circuit, individual peripherals or memory. The AHB and APB clock supports dynamic clock slow down or gating when bus fabric is idle.
- **System clock source** — four different clock sources can be used to drive the master clock (F_{CPU} and F_{MEMS}):
  - 26MHz Digitally Controlled Crystal Oscillator (DCXO) that can supply reference clock for PLLs.
  - Main PLL (MPLL) fed by reference clock from UPLL that in turn is fed by DCXO, with a maximum frequency at 624MHz.
  - Low Frequency RC oscillator (LFOSC) — Low power consumption with large frequency variation.
  - High Frequency RC oscillator (HFOSC) — Low power consumption with large frequency variation.
- **Auxiliary clock source** — Three low power clock sources to drive the real-time clock. In 32k-less mode, DCXO32K and EOSC32K are used, while in 32k mode only XOSC32K is used:
  - 32.768kHz low-speed external crystal (XOSC32K).
  - 32.768kHz low-speed internal clock fed by DCXO (DCXO32K).
  - 32.768kHz low-speed internal RC (EOSC32K) with larger frequency variation compared to DCXO and XOCS.
- **Peripheral clock sources** — Three types of peripheral clock source options are used. Each peripheral has its own gating register:
  - Peripherals, such as USB, MSDC, UARTs, DSP, LCD and SFC have their own independent clock based on the system clock. HFOSC and MPLL, each having independent outputs enabling high flexibility, can generate independent clocks for MSDC, DSP, LCD and SFC. UPLL can generate independent clocks for USB.
  - Clock of peripherals, such as I2C_D2D, I2C2, DMA, DMA_AO, SPISLV and BTIF is the same as AHB2/APB2 bus clock (F_{PERI}).
  - Clock of multi-media related peripherals, such as G2D, RESIZER, ROTDMA and DSI is the same as AHB1/APB1 bus clock (F_{MEMS}).

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  - Clock of low-speed peripherals, such as I2C0, I2C1, SPI, SENSOR_DMA, AUXADC and EFUSE is from general 26MHz MUX.

- **Clock-out capability.**
  - F_{REF}. Outputs DCXO 26MHz clock by control GPIO45.
  - CLK_{OUT}. Outputs 32.768kHz clock based on 32k or 32k-less mode.

26MHz DCXO is selected as a default CPU clock when powering up or resetting the chip. This clock source serves as an input to a set of cascaded PLLs (UPLL and MPLL) to increase the CPU frequency (FCPU) up to 208MHz when VCORE is 1.3V. The application can then select the system clock as either Low Frequency RC oscillator (LFOSC) or High Frequency RC oscillator (HFOSC) to decrease power consumption while frequency variation is acceptable. LFOSC can provide maximum of 26MHz clock while HFSOC can provide maximum of 312MHz clock. CPU can switch to HFOSC 104MHz as DVFS option while working at VCORE 1.1V. Several prescalers allow the configuration of the memory domain AHB buses. The maximum frequency of the AHB1 and APB1 buses (FMEMS) is 104MHz. The maximum frequency of peripheral AHB2 and high-speed APB2 buses (FPERI) is 62.4MHz, while the maximum frequency of the low-speed APB3 domains is 26MHz. The frequency ratio of FCPU and FMEMS needs to be 2:1. When VCORE is 0.9V, the maximum frequency of the FCPU is 26MHz, FMEMS and FPERI are at 13MHz. The device has dedicated BTPLL and MIPIPLL to operate Bluetooth and MIPI.

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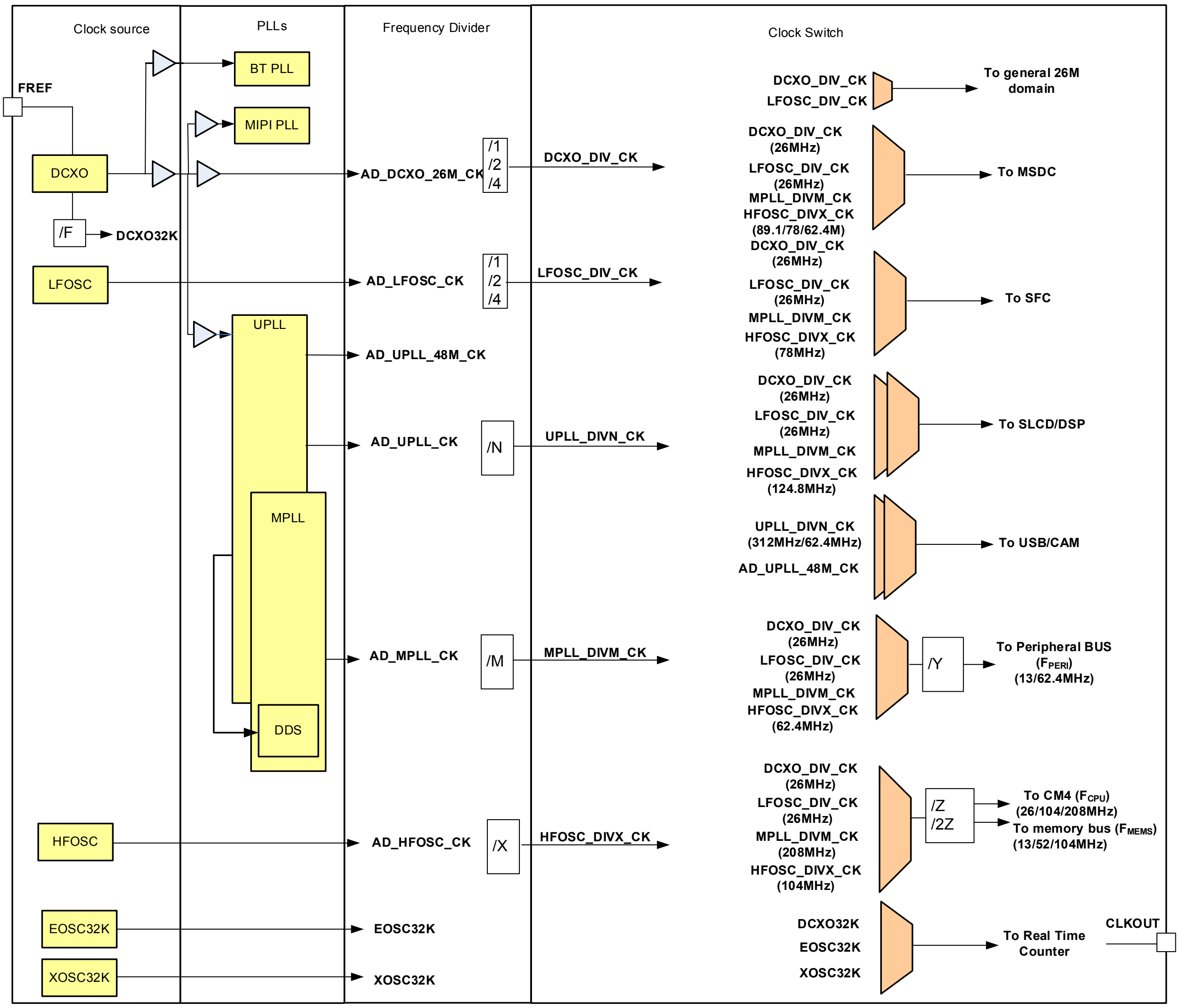

Figure 2.3-1. MT2533D clock source architecture

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2.4. Communication Interface

2.4.1. Universal Asynchronous Receiver Transmitter

MT2533D chipset houses four Universal Asynchronous Receivers/Transmitters (UARTs). UARTs provide full duplex serial communication channel between the baseband chipset and external devices. The UART has both M16C450 and M16550A modes of operation compatible with a range of standard software drivers.

UARTs support baud rates from 110bps up to 921,600bps with a baud rate auto-detection function. They provide hardware and software flow control of the RTS/CTS signals.

UARTs can configure data transfer lengths from 5 to 8 bits, with an optional parity bit and one or two stop bits by software. They can be served by the DMA controller.

2.4.2. Serial Peripheral Interface

MT2533D chipset features four Serial Peripheral Interface (SPI) master controllers and one SPI slave controller to receive/transmit device data using SPI protocol. The SPI controllers can communicate at up to 13 Mbps. SPI master controllers support two chip select outputs to connect the controller to two devices simultaneously.

The chip select signal and SPI clock of SPI master controllers are configurable. The SPI controllers also support DMA mode for large numbers of data transmissions.

2.4.3. Inter-Integrated Circuit Interface

MT2533D chipset provides three Inter-Integrated Circuit Interface (I2C) master controllers. There are three types of speed modes in the I2C controllers: standard mode (100kbit/s), fast mode (400kbit/s) and high-speed mode (3.4Mbit/s), supporting 7-bit/10-bit addressing and can be served by the DMA controller. The I2C package size supports up to 65,535 bytes per transfer and 255 transfers per transaction in DMA mode and 8 bytes per transfer in non-DMA mode. START/STOP/REPEATED START condition can be increased to support single or multi transfer. These features can be configured by software upon our customers' requirements.

2.4.4. SD Memory Card Controller

The controller fully supports the SD memory card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0.

Furthermore, the controller also partially supports the SDIO card specification version 2.0. However, the controller can only be configured as the host of the SD memory card. Hereafter, the controller is abbreviated as the SD controller.

Main features of the controller:

- 16 or 32-bit access for control registers.
- Built-in CRC circuit.
- CRC generation can be disabled.
- Supports DMA.
- Data rate of up to 48 Mbps in serial mode, 48 x 4Mbps in parallel model. The module is targeted at 48MHz operating clock.
- The serial clock rate on SD bus is programmable.
- Card detection capability in sleep mode.

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- Power control for memory card.

2.4.5. USB2.0 high-speed device controller

USB2.0 controller supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) modes. USB2.0 controller provides two endpoints to receive packets and four endpoints to send packets. These endpoints can be individually configured in the software to handle either bulk transfers, interrupt transfers or isochronous transfers. There are four DMA channels, and the embedded RAM size is configurable up to 3,264 bytes. The embedded RAM can be dynamically configured for each endpoint. For more details, see Table 2.4-1.

Table 2.4-1. USB2.0 features

Feature	Description
Speed	HS (480MHz)/FS (12MHz)/LS (1.5MHz)
Enhanced feature	Generic device
Endpoint	4TX/2RX
DMA channel	4
Embedded RAM	3264 bytes

2.5. Peripherals

2.5.1. Pulse-Width Modulation

There are six Pulse-Width Modulation (PWM) controllers to generate pulse signals. The duty cycle, high time and low time of pulse signals can be programmed. The PWM controllers support both 13MHz and 32.768kHz clock sources to increase the operating range by software configuration.

2.5.2. General Purpose Inputs/Outputs

Each of the General Purpose Inputs/Outputs (GPIO) pins are software configurable as an output (push-pull or open-drain) or input (with or without pull-up or pull-down) that supports floating input with buffer gating to reduce power consumption. Most of the GPIO pins are multiplexed with peripheral functions and have selectable output driving strength. Fast I/O signal transmission allows maximum I/O toggling speed of up to 100MHz. Besides, I/O toggling is allowed even when the chip operates in deep sleep mode with a voltage of 0.7V.

2.5.3. Keypad scanner

MT2533D platform provides a keypad hardware module. The keypad supports two types of keypads: 3 x 3 single keys and 3 x 3 configurable double keys.

The 3 x 3 keypad supports a matrix with 3*3*2 = 18 keys. The 18 keys are divided into 9 subgroups, and each group consists of two keys and a 20Ω resistor. The keypad de-bounce time can be configured for your operation.

2.5.4. General Purpose Timer

The general purpose timer (GPT) includes five 32-bit timers and one 64-bit timer. Each timer has four operation modes, which are **ONE-SHOT**, **REPEAT**, **KEEP-GO** and **FREERUN**, and can operate on one of the two clock sources; RTC clock (32.768kHz) and system clock (13MHz).

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2.5.5. Real Time Clock

The Real Time Clock (RTC) module provides time and data information, as well as 32.768kHz clock. The 32.768kHz clock is selected from the external XTAL (XOSC32) clock source. The RTC block has an independent power supply. When the MT2533D platform is powered off, a dedicated regulator will supply power to the RTC block. In addition to providing timing data, an alarm interrupt will be generated and can be used to power up the baseband core. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches the maximum value. The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

2.5.6. True Random Number Generator

The True Random Number Generator (TRNG) is a device in power-down domain that generates 32 bits random numbers based on the ring oscillator output that is sensitive to the PVT (process, voltage, temperature) variation. The utilized ring oscillator includes Hybrid Fibonacci Ring Oscillator (H-FIRO), Hybrid Ring Oscillator (H-RO) and Hybrid Galois Ring Oscillator (H-GARO). Von Neumann extractor is used to balance the 0/1 probability of the generated random numbers. Error detection detects if the generation time exceeds the timeout limit while enabling the Von Neumann extractor. IRQ is issued when random number is successfully generated or timeout error occurs.

2.5.7. General Purpose Counter

The general purpose counter (GPC) is to count the signal toggle times of chip I/O, and calculate the frequency and duration. It counts once the channel is enabled and provides an interrupt switch trigger when the counter exceeds the threshold. The threshold can be configured by software.

2.5.8. Accessory detector

The accessory detector (ACCDET) detects the plug-in and plug-out of multiple types of external components. This design supports two types of external components, microphone and hook-switch. It uses an internal 2-bit comparator to separate external components. The de-bounce scheme is also supported to resist uncertain input noises.

2.6. Analog baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the data transfer to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete analog baseband signal processing:

1) Auxiliary ADC. Provides an ADC for battery and other auxiliary analog function monitoring.
2) Audio mixed-signal block. Provides complete analog voice signal processing, including microphone amplification, A/D conversion, D/A conversion, earphone driver, etc. Dedicated stereo D/A conversion and amplification for audio signals are also included.
3) Clock generation. Includes a clock squarer for shaping the system clock and PLL to provide clock signals to MCU and USB.
4) XOSC32. A 32.768kHz crystal oscillator circuit for RTC applications on analog blocks.
5) LPOSC. Provides 26MHz and 312MHz system clocks for low power applications.

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2.6.1. Auxiliary ADC

2.6.1.1. Block description

The auxiliary ADC includes the following functional blocks:

1) Analog multiplexer. Selects a signal from one of the seven auxiliary input pins. Real-world messages are monitored, such as temperature and transferred to the voltage domain.

2) 12-bit A/D converter: Converts the multiplexed input signal to 12-bit digital data.

Table 2.6-1. Auxiliary ADC input channel

Channel	Application	Input range [V]
11~15	GPIO	0 to 2.8
others	Internal use	N/A

2.6.1.2. Functional specifications

The functional specifications of the auxiliary ADCs are listed in Table 2.6-2.

Table 2.6-2. Auxiliary ADC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution	-	12	-	Bit
FC	Clock rate	-	1.08	-	MHz
FS	Sampling rate at N-Bit	-	1.08/(N+1)	-	MSPS
	Input swing	0	-	2.8	V
CIN	• Input capacitance ○ Unselected channel ○ Selected channel	 - -	 - -	 50 4	 fF pF
RIN	• Input resistance ○ Unselected channel ○ Selected channel	 400 1	 - -	 - -	 MΩ MΩ
	Clock latency	-	N+1	-	1/FC
DNL	Differential nonlinearity	-	± 1	-	LSB
INL	Integral nonlinearity	-	± 1	-	LSB
OE	Offset error	-	± 10	-	mV
FSE	Full swing error	-	± 10	-	mV
SINAD	Signal to noise and distortion ratio (10kHz full swing input and 1.0833-MHz clock rate)	-	65	-	dB
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
	• Current consumption				

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	○ Power-up	-	280	-	µA
	○ Power-down	-	1	-	µA

2.6.2. Audio mixed-signal blocks

2.6.2.1. Block description

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. It includes three parts, as shown in Figure 2.6-1. The first part consists of stereo audio DACs and audio amplifiers for audio playback. The second part is the voice downlink path, including voice-band DACs (left channel audio DAC) and voice amplifier that produces voice signals to earphones or other auxiliary output devices. The last part is the voice uplink path — an interface between the microphone or other auxiliary input devices and the MT2533D chipset. A set of bias voltage is provided for the external electric microphone.

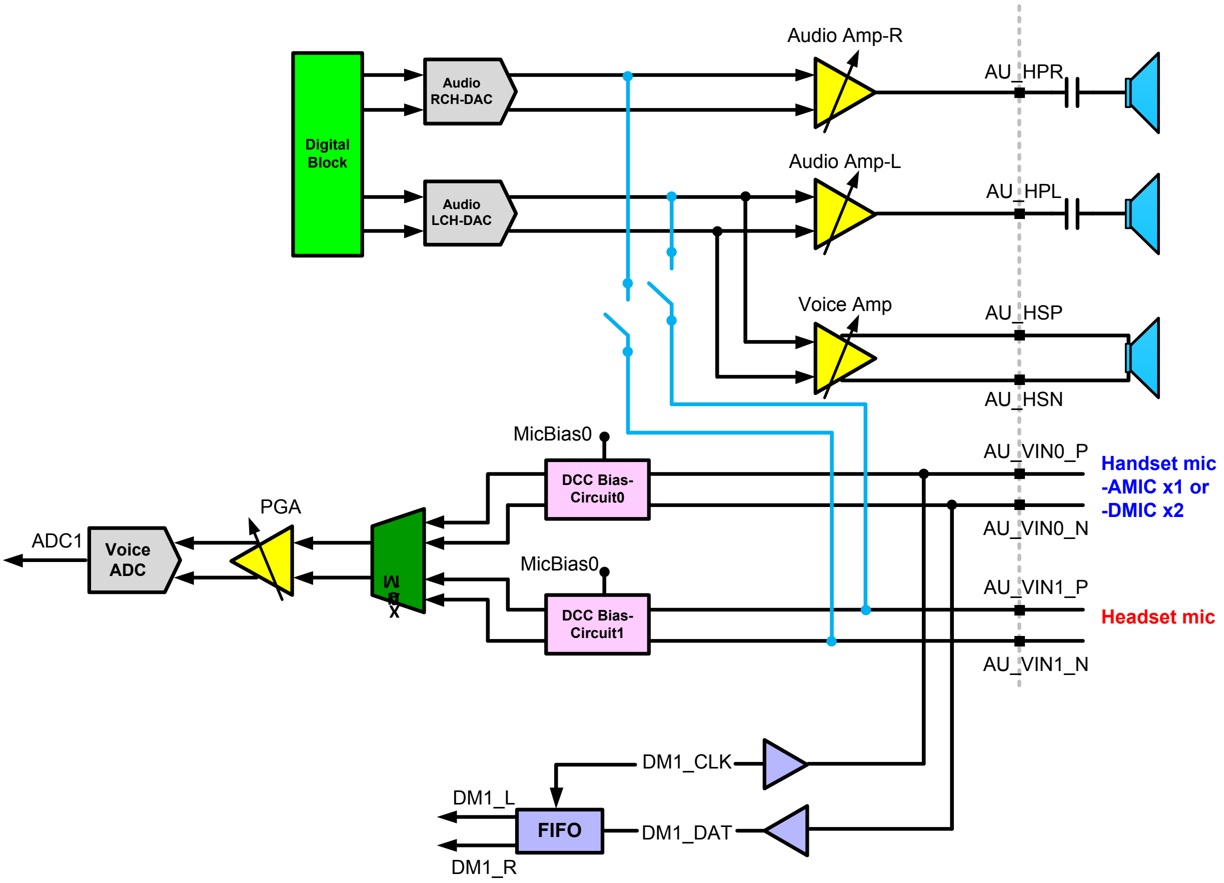

Figure 2.6-1. Block diagram of audio mixed-signal blocks

2.6.2.2. Functional specifications

See Table 2.6-3 for the functional specifications of voice-band uplink/downlink blocks.

Table 2.6-3. Functional specifications of analog voice blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit

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Symbol	Parameter	Min.	Typ.	Max.	Unit
FS	Sampling rate	-	6,500	-	kHz
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
VMIC	Microphone biasing voltage	-	1.9	2.2	V
IMIC	Current draw from microphone bias pins	-	-	2	mA
Uplink path					
IDC	Current consumption for one channel	-	1.5	-	mA
SINAD	Signal to noise and distortion ratio Input level: -40 dbm0 Input level: 0 dbm0	 29 -	 - 69	 - -	 dB dB
RIN	Input impedance (differential)	13	20	27	kΩ
ICN	Idle channel noise	-	-	-67	dBm0
Downlink path					
IDC	Current consumption	-	2.2	-	mA
SINAD	Signal to noise and distortion ratio Input level: -40 dBm0 Input level: 0 dBm0	 29 -	 - 69	 - -	 dB dB
RLOAD	Output resistor load (differential)	16	32	-	Ω
CLOAD	Output capacitor load	-	-	250	pF
ICN	Idle channel noise of transmit path	-	-	-64	dBPa
XT	Crosstalk level on transmit path	-	-	-66	dBm0
Digital MIC					
DCLK	DMIC clock frequency	-	3.25/ 1.625	-	MHz
DTY	DMIC clock duty cycle	40	-	60	%
DCRT	DMIC clock rise time (MaxCL = 65p)	-	-	10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)	-	-	10	ns

See Table 2.6-4 for functional specifications of audio blocks.

Table 2.6-4. Functional specifications of analog audio blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FCK	Clock frequency	-	6.5	-	MHz
Fs	Sampling rate	32	44.1	48	kHz
AVDD	Power supply	2.6	2.8	3.0	V

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Symbol	Parameter	Min.	Typ.	Max.	Unit
T	Operating temperature	-40	-	85	°C
IDC	Current consumption	-	2.2	-	mA
PSNR	Peak signal to noise ratio	-	88	-	dB
DR	Dynamic range	-	88	-	dB
VOUT	Output swing for 0dBFS input level at -1dB headphone gain	-	0.707	-	V_{rms}
$VOUT_{MAX}$	Maximum output swing	-	2.0	-	V_{pp}
THD	Total harmonic distortion 10mW at 64Ω load	-	-	-70	dB
RLOAD	Output resistor load (single-ended)	64	-	-	Ω
CLOAD	Output capacitor load	-	-	250	pF
XT	L-R channel cross talk	70	-	-	dB

2.6.3. Phase Locked Loop and oscillators

2.6.3.1. Block description

There are two phase-locked loops (PLL) in PLLGP. The UPLL generates 624MHz clock output, and then a frequency divider generates fixed 48MHz clock. The DDS-based MPLL is with target/highest frequency of 624MHz (hopping range is from -8% to 0%, and the frequency is from 574MHz to about 624MHz). These two PLLs do not require off-chip components to operate, and can be turned off to save power. Figure 2.6-2 shows the block diagram of clock sources.

After powering on, the PLLs are all off by default control register setting, and the source clock signal is selected through multiplexers from 26MHz XTAL. The software maintains the PLL lock time while the clock selection is changing.

There is one high frequency low power oscillator (HFOSC) and one low frequency low power oscillator (LFOSC) in low power oscillator (LPOSC) group. The HFOSC generates 312MHz clock output with from -13% to 0% frequency variation. The LFOSC generates 26MHz clock output with from -8% to 0% variation. The software calibrates two LFOSC by frequency meter before using them.

Note that PLLs and LPOSC need some time to stabilize after powering on. The software maintains the PLL and LPOSC lock time before switching them to the proper frequency. Usually, a software loop longer than the PLL and LPOSC lock time is employed when the PLL lock time is too long.

For power management, the MCU software configuration may stop MCU Clock by setting up the Sleep Control Register. Any interrupt requests to MCU can pause the sleep mode and return the MCU to the running mode.

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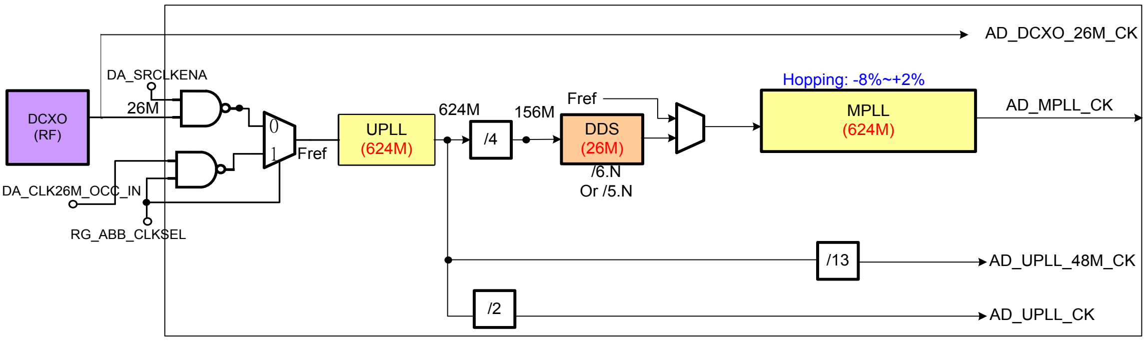

Figure 2.6-2. Block diagram of PLL clock sources

2.6.3.2. Function specifications

The function specifications of PLLs and oscillators are shown in Table 2.6-5,

Table 2.6-6,

Table 2.6-7,

Table 2.6-8 and Table 2.6-9.

Table 2.6-5. MPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	-	26	-	MHz
Fout	Output clock frequency	420	624	740	MHz
	Settling time	-	20	-	µs
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)	-	30	-	ps
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
	Current consumption	-	1.8	-	mA
	Power-down current consumption	-	-	0.5	µA

Table 2.6-6. UPLL specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	-	26	-	MHz
Fout	Output clock frequency	420	624	740	MHz

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Settling time	-	20	-	µs
	Output clock duty cycle	45	50	55	%
	Output clock jitter (period jitter)	-	30	-	ps
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
	Current consumption	-	1.8	-	mA
	Power-down current consumption	-	-	0.5	µA

Table 2.6-7. DDS specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fin	Input clock frequency	-	156	-	MHz
Fout	Output clock frequency	-	26	-	MHz
	Settling time	-	20	-	µs
	Output clock duty cycle	47	50	53	%
	Output clock jitter (period jitter)	-	60	-	ps
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-40	-	85	°C
	Current consumption	-	0.8	-	mA
	Power-down current consumption	-	-	0.5	µA

Table 2.6-8. HFOSC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency	272	287	312	MHz
	Settling time		3.5		µs
	Output clock duty cycle	40	50	60	%
	Output clock jitter (period jitter)		150		ps
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-40	-	85	°C

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Symbol	Parameter	Min.	Typ.	Max.	Unit
	Current consumption	-	0.1	-	mA
	Power-down current consumption	-	-	5	µA

Table 2.6-9. LFOSC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fout	Output clock frequency (after calibration)	24	25	26	MHz
	Settling time	-	3.5	-	µs
	Output clock duty cycle	40	50	60	%
	Output clock jitter (period pk-topk jitter)	-	250	-	ps
DVDD	Digital power supply	-	1.1	-	V
AVDD	Analog power supply	1.7	1.8	1.9	V
T	Operating temperature	-40	-	85	°C
	Current consumption	-	0.05	-	mA
	Power-down current consumption	-	-	5	µA

2.7. Audio front-end

The audio front-end essentially consists of voice and audio data paths. Mono hands-free audio or external FM radio playback paths are also provided. The audio stereo path facilitates CD-quality playback, external FM radio, and voice playback through a headset.

Figure 2.7-1. Figure 2.7-1 shows the block diagram of the audio front-end digital circuits. The APB register block is an APB peripheral that stores settings from the MCU. The DSP audio port (DAP) block interfaces with the DSP for control and data communication. The digital filter block performs filter operations for voice band and audio band signal processing. The Digital Audio Interface (DAI) block communicates with the system simulator for FTA or external Bluetooth or codec modules.

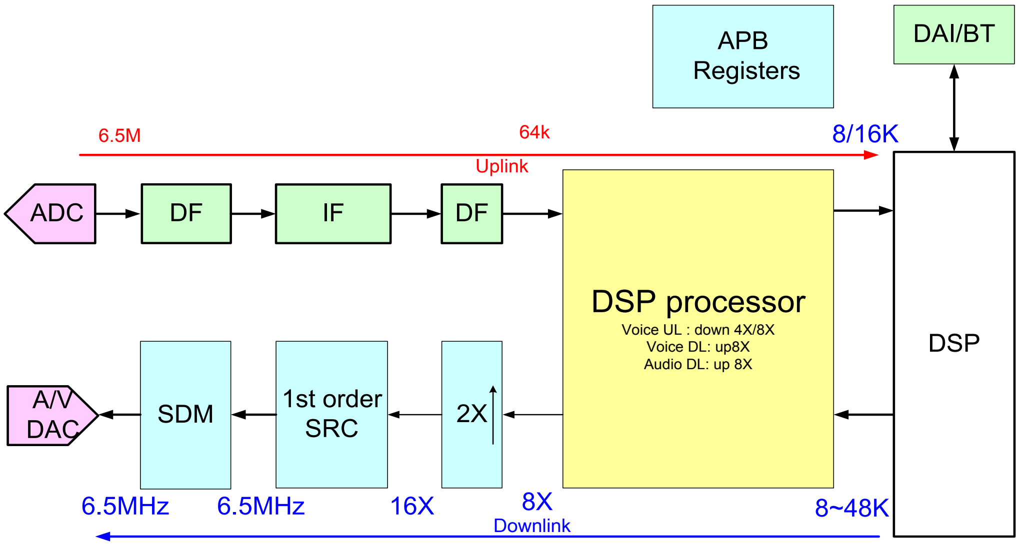

Figure 2.7-1. Digital circuits of the audio front-end

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To communicate with the external Bluetooth module, the master-mode PCM interface and master-mode I2S/EIAJ interfaces are supported. The clock of PCM interface is at 256kHz while the frame synchronization is at 8kHz. Both long synchronization and short synchronization interfaces are supported. The PCM interface can transmit 16-bit stereo or 32-bit mono 8kHz sampling rate voice signal. Figure 2.7-2 shows the timing diagram of the PCM interface. Note that the serial data changes when the clock is on rising edge and data is latched when the clock is on falling edge. Figure 2.7-3 shows the timing diagram of PCM interface for different clock rates. The clock rate could be configured to 1, 2, 4 or 8 times of the original clock rate.

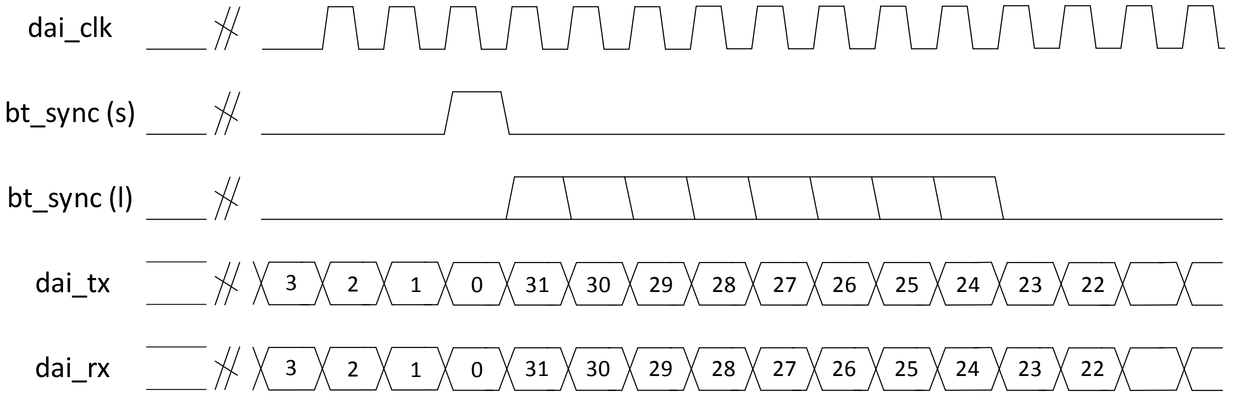

Figure 2.7-2. Timing diagram of Bluetooth application

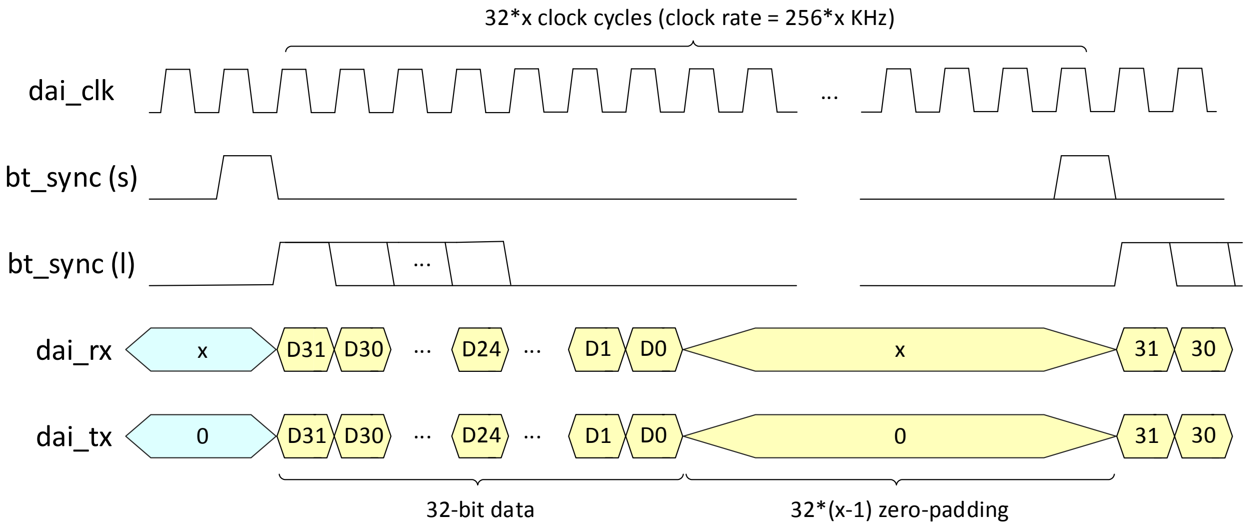

Figure 2.7-3. Timing diagram of different clock rate Bluetooth applications

I2S/EIAJ interface is designed to transmit high quality audio data. Figure 2.7-4 and Figure 2.7-5 illustrate the timing diagram of the two types of interfaces. The I2S/EIAJ supports audio signals with 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz and 48kHz sampling rates. The clock frequency of I2S/EIAJ can be 32 × (sampling frequency), or 64 × (sampling frequency). For example, to transmit 44.1kHz CD-quality music, the clock frequency should be 32 × 44.1 kHz = 1.4112MHz or 64 × 44.1 kHz = 2.8224MHz.

I2S/EIAJ interface is not only used for Bluetooth module, but also for external DAC components. The audio data can be sent to the external DAC through the I2S/EIAJ interface.

In this document, the I2S/EIAJ interface is referred to as External DAC Interface (EDI).

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Table 2.7-1 shows the DAI and EDI clock jitter percentages. The jitter period of the DAI/EDI clock is almost fixed, because of the power saving implementation of the hardware. Therefore, the jitter percentage will increase by increasing the audio sampling rate (or decreasing the clock period).

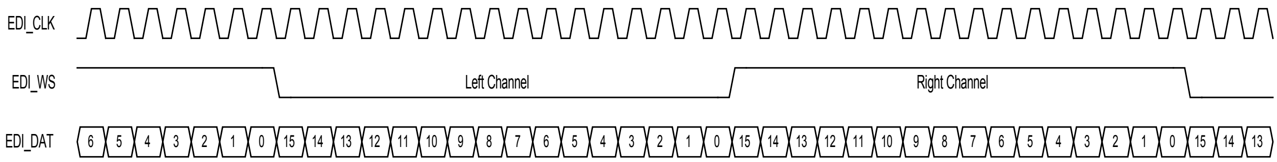

Figure 2.7-4. EDI Format 1: EIAJ (FMT = 0)

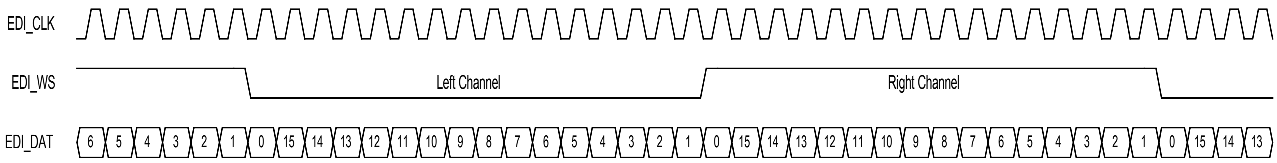

Figure 2.7-5. EDI Format 1: I2S (FMT = 1)

Table 2.7-1. Clock jitter of DAI and EDI

Clock jitter at 1X clock rate		
Frequency (kHz)	**PCM**	**I2S**
8.000	2.56%	2.56%
11.025	N/A	3.53%
12.000	N/A	3.84%
16.000	N/A	5.12%
22.050	N/A	7.06%
24.000	N/A	7.68%
32.000	N/A	10.24%
44.100	N/A	14.11%
48.000	N/A	15.36%

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3. Bluetooth RF Subsystem

3.1. Bluetooth description

The Bluetooth RF subsystem (see Figure 3.1-1) contains a fully integrated transceiver with on-chip RF bandpass filter (BPF).

For transmitter (TX) path, the baseband data are digitally modulated in the baseband processor and then up-converted to 2.4GHz RF channels through DA converter, filter, IQ up-converter and power amplifier. The power amplifier is capable of transmitting 5dBm power for enhanced data rate (EDR) and 8dBm for basic data rate (BDR).

MT2533D Bluetooth module has low intermediate frequency (IF) receiver architecture. RF signal is amplified by LNA and down-converted to IF by mixer. LO is provided by synthesizer, which supports 26MHz reference clock. The mixer output is filtered by complex BPF and then converted to digital signal by ADC. A fast automatic gain control (AGC) enables effective discovery of devices within dynamic range of the receiver.

BBPLL generates a sampling clock for ADC and DAC.

MT2533D Bluetooth module features self-calibration schemes to compensate the variation of process and temperature to maintain high performance. Those calibrations are performed automatically right after system boot-up.

Note, the specification value is valid at room temperature (25°C).

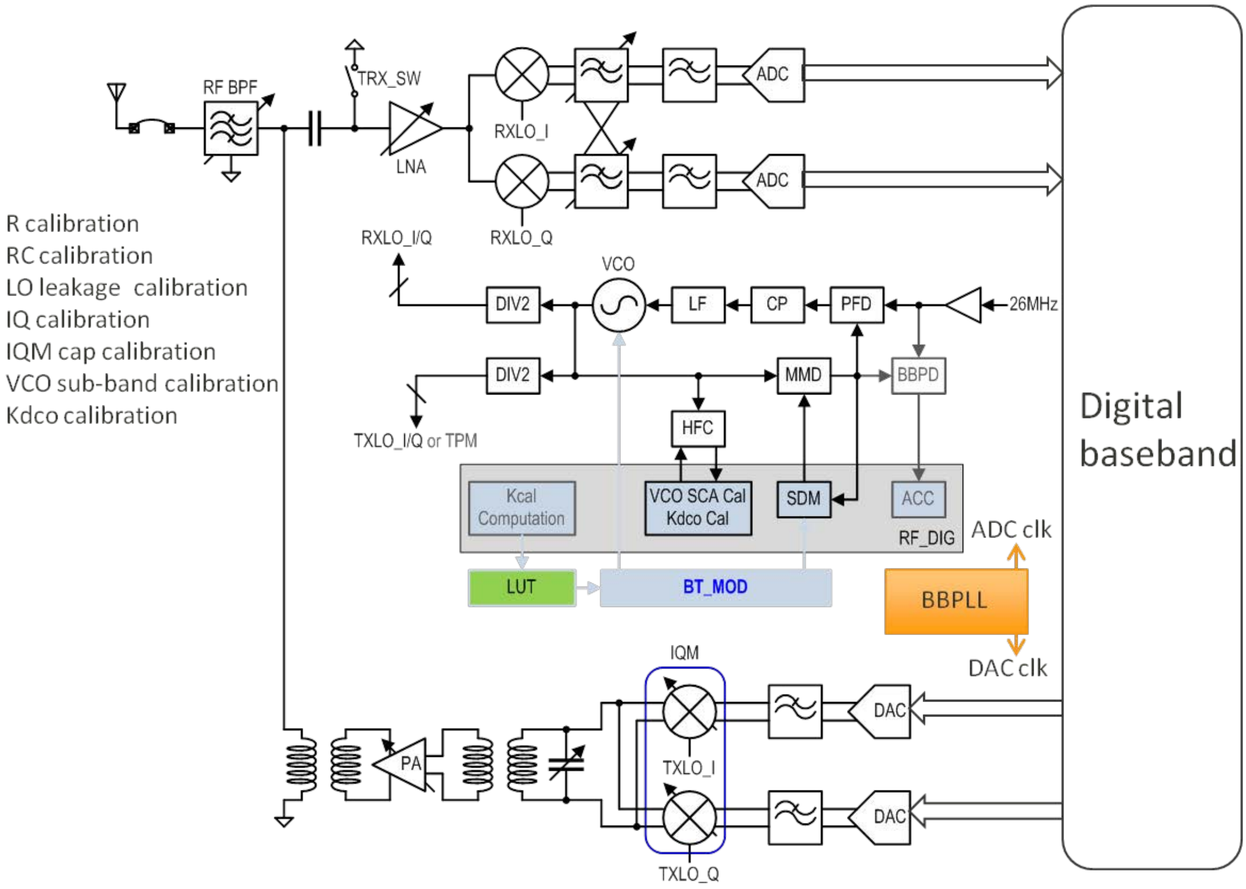

Figure 3.1-1. Bluetooth RF transceiver system

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3.2. Functional specifications

3.2.1. Basic Data Rate – receiver specifications

Table 3.2-1. Basic Data Rate – receiver specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	BER < 0.1% (DH5)	-	-93	-70	dBm
Max. detectable input power	BER < 0.1%	-20	-5	-	dBm
C/I co-channel selectivity	BER < 0.1%	-	6	11	dB
C/I 1 MHz adj. channel selectivity	BER < 0.1%	-	-7	0	dB
C/I 2 MHz adj. channel selectivity	BER < 0.1%	-	-40	-30	dB
C/I ≥ 3 MHz adj. channel selectivity	BER < 0.1%	-	-43	-40	dB
C/I image channel selectivity	BER < 0.1%	-	-20	-9	dB
C/I image 1 MHz adj. channel selectivity	BER < 0.1%	-	-35	-20	dB
Out-of-band blocking	30 to 2,000 MHz	-10	-4	-	dBm
	2,000 to 2,350 MHz	-27	-14	-	dBm
	2,350 to 2,400 MHz	-27	-18	-	dBm
	2,500 to 2,550 MHz	-27	-18	-	dBm
	2,550 to 3,000 MHz	-27	-14	-	dBm
	3,000 MHz to 12.75 GHz	-10	1	-	dBm
Intermodulation		-39	-30	-	dBm

3.2.2. Basic Data Rate – transmitter specifications

Table 3.2-2. Basic Data Rate – transmitter specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Maximum transmit power		-	8	-	dBm
Gain step		2	4	8	dB
Δf1avg (00001111)		140	157	175	kHz
Δf2max (10101010)		115	122	-	kHz
Δf1avg/Δf2avg		0.8	0.9	-	kHz
Initial carrier frequency drift		-75	10	75	kHz
Frequency drift	DH1	-25	15	25	kHz
	DH3	-40	18	40	kHz
	DH5	-40	18	40	kHz

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Description	Condition	Min.	Typ.	Max.	Unit
Maximum drift rate		-	9		kHz/µs
BW 20dB of TX output spectrum		-	920	1,000	kHz
In-band spurious emission	±2 MHz offset	-	-38	-20	dBm
	±3 MHz offset	-	-43	-40	dBm
	> ±3 MHz offset	-	-43	-40	dBm
Out-of-band spurious emission	30 MHz to 1 GHz	-	-	-36	dBm
	1 to 12.75 GHz	-	-	-30	dBm
	1.8 to 1.9 GHz	-	-	-47	dBm
	5.15 to 5.3 GHz	-	-	-47	dBm

3.2.3. Enhanced Data Rate – receiver specifications

Table 3.2-3. Enhanced Data Rate – receiver specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	π/4 DQPSK, BER < 0.01% (2DH5)	-	-93	-70	dBm
	8PSK, BER < 0.01%	-	-87	-70	dBm
Maximum detectable input power	π/4 DQPSK, BER < 0.01% (3DH5)	-20	-5	-	dBm
	8PSK, BER < 0.01%	-20	-5	-	dBm
C/I co-channel selectivity	π/4 DQPSK, BER < 0.01%	-	9	13	dB
	8PSK, BER < 0.01%	-	16	21	dB
C/I 1MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-12	0	dB
	8PSK, BER < 0.01%	-	-6	5	dB
C/I 2MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-40	-30	dB
	8PSK, BER < 0.01%	-	-36	-25	dB
C/I ≥ 3MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-43	-40	dB
	8PSK, BER < 0.01%	-	-40	-33	dB
C/I image channel selectivity	π/4 DQPSK, BER < 0.01%	-	-20	-7	dB
	8PSK, BER < 0.01%	-	-15	0	dB
C/I image 1 MHz adj.	π/4 DQPSK, BER < 0.01%	-	-40	-20	dB

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Description	Condition	Min.	Typ.	Max.	Unit
channel selectivity	8PSK, BER < 0.01%	-	-30	-13	dB

3.2.4. Enhanced Data Rate – transmitter specifications

Table 3.2-4. Enhanced Data Rate – transmitter specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Max. transmit power	π/4 DQPSK	-	5	-	dBm
	8PSK	-	5	-	dBm
Relative transmit power	π/4 DQPSK	-4	-1.5	1	dB
	8PSK	-4	-1.5	1	dB
Freq. stability ω0	π/4 DQPSK	-10	4	10	kHz
	8PSK	-10	4	10	kHz
Freq. stability ω1	π/4 DQPSK	-75	20	75	kHz
	8PSK	-75	20	75	kHz
| ω0+ω1|	π/4 DQPSK	-75	20	75	kHz
	8PSK	-75	20	75	kHz
RMS DEVM	π/4 DQPSK	-	8	20	%
	8PSK	-	8	13	%
99% DEVM	π/4 DQPSK	-	12	30	%
	8PSK	-	12	20	%
Peak DEVM	π/4 DQPSK	-	17	35	%
	8PSK	-	17	25	%
In-band spurious emission	π/4 DQPSK, ±1 MHz offset	-	-33	-26	dBm
	8PSK, ±1 MHz offset	-	-33	-26	dBm
	π/4 DQPSK, ±2 MHz offset	-	-30	-20	dBm
	8PSK, ±2 MHz offset	-	-30	-20	dBm
	π/4 DQPSK, ±3 MHz offset	-	-43	-40	dBm
	8PSK, ±3 MHz offset	-	-43	-40	dBm

Note: To meet the specifications, use a front-end band-pass filter.

3.2.5. Bluetooth LE – receiver specifications

Table 3.2-5. Bluetooth LE – receiver specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Receiver sensitivity	BER < 30.8%	-	-96.5	-70	dBm
Maximum detectable input power	BER < 30.8%	-10	-5	-	dBm
C/I co-channel selectivity	BER < 30.8%	-	6	21	dB

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Description	Condition	Min.	Typ.	Max.	Unit
C/I 1 MHz adj. channel selectivity	BER < 30.8%	-	-7	15	dB
C/I 2 MHz adj. channel selectivity	BER < 30.8%	-	-30	-17	dB
C/I ≥ 3 MHz adj. channel selectivity	BER < 30.8%	-	-33	-27	dB
C/I image channel selectivity	BER < 30.8%	-	-20	-9	dB
C/I image 1 MHz adj. channel selectivity	BER < 30.8%	-	-30	-15	dB
Out-of-band blocking	30MHz to 2,000MHz	-	-	-30	dBm
	2,001MHz to 2,339MHz	-	-	-35	dBm
	2,501MHz to 3,000MHz	-	-	-35	dBm
	3,001MHz to 12.75GHz	-	-	-30	dBm

3.2.6. Bluetooth LE – transmitter specifications

Table 3.2-6. Bluetooth LE – transmitter specifications

Description	Condition	Min.	Typ.	Max.	Unit
Frequency range		2,402	-	2,480	MHz
Output power		-20	0	-	dBm
Modulation characteristics	Δf1avg (00001111)	235	250	265	kHz
	Δf2max (10101010)	185	215	-	kHz
	Δf1avg/Δf2avg	0.8	0.9	-	kHz
Carrier frequency offset and drift	Frequency offset	-150	±5	150	kHz
	Frequency drift	-50	±5	50	kHz
	Max. drift rate	-20	±3	20	kHz/µs
In-band spurious emission	±2 MHz offset	-	-35	-20	dBm
	±3 MHz offset	-	-40	-30	dBm
	> ±3 MHz offset	-	-40	-30	dBm

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4. Digital Signal Processing

4.1. Hardware features

- 128kB IRAM, 250kB DRAM, 96kB SRAM with Auto Voice Buffer Scheme.
  - Provides more than 3 seconds of dual voice buffer for seamless operation.
  - Auto Voice Buffers are built for MICs, DAC/TXs and RXs, to prevent overhead from context switch of DSP interrupts. Each MIC, DAC/TX, RX has its auto buffer. Programmable.
- Programmable LDO (from 0.9 to 1.32V) and PLL (from 1MHz to 150+MHz), for MIPS and power requirements.
- Supports various sampling rates: 8, 16, 24, 32, 44.1, 48kHz.
- Supports two PDM_DATA inputs (support up to 4 Digital MICs) and two PDM_DATA output pins.
- Supports two TX (microphone) and one RX (AEC reference) of I2S.
- Microphone output can be in I2S or PDM format.
- 32kHz, 512kHz, 768kHz and 1MHz PDM_CLKO with 16kHz sampling rate in power saving mode.
- Built-in pull up resistors for SCL_H, and SDA_H.
- SPI/I2C for program and acoustic model download at speeds of up to 20MHz/400kHz.
- AVD to provide ultra-low current for wakeup operation.

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5. Low Power Control System

5.1. MTCMOS power domain

The MTCMOS technology is adopted to reduce the power consumption according to different scenarios. Table 5.1-1 provides the list of MTCMOS partitions. Each domain can be optionally turned on and off by software control.

Table 5.1-1. The MTCMOS power domain

MTCMOS domain	Description
AO_PD	Always on power domain. To save the power, only limited resources such as wakeup logics and modules that should keep register retention are designed in this domain.
INFRA_PD	The Infrasys MTCMOS domain. The major bus fabric and peripheral designs, such as I2C, UART, PWM, SPI, DMA and USB, are in this domain.
CPU_PD	CPU MTCMOS domain. The CPU core, cache controllers with ROM and RAM. This MTCMOS domain contains Cortex-M4 core and the cache controller with ROM and SRAM. It will power-off only in sleep or deep sleep mode.
MMSYS_PD	Multimedia system MTCMOS domain. The display engine, 2D graphic engine and image processing unit are in this domain.
BT_AO_PD	BT_AO MTCMOS domain. Circuits that belong to Bluetooth/Bluetooth LE/ANT are designed in this domain.
BT_OFF_PD	BT_OFF MTCMOS domain. Circuits that belong to BT/BLE/ANT are designed in this domain.
DSP_PD	DSP MTCMOS domain. The FD216 DSP with ROM and RAM and the audio interface (I2S, PCM and MIC) are supported in this domain.

5.2. Power modes

Different power modes are designed to optimize the current consumption further. Table 5.2-1 summarizes the power modes and peripheral usage.

Table 5.2-1. Power modes

Feature	Configurable power mode				
	High-Speed	Full-Speed	Low-Speed	Sleep	PowerOff
CPU	Active	Active	Active	Off	Off
CPU Frequency	208Mhz	104Mhz	26Mhz	Off	Off
BUS Frequency	62.4Mhz	62.4Mhz	13M	Off	Off
Flash	On	On	On	PowerDown	Off

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Feature	Configurable power mode				
PSRAM	On	On	On	HalfSleep [(1)]	Off
SRAM	On	On	On	Retention/Off	Off
MCU Clock Source	PLL	HFOSC	DCXO/LFOSC	Off	Off
RTC	On	On	On	On	On
Wakeup time[(2)]	–	–	–	LowSpeed: 7μs Others: 320μs	50ms

1) **Active mode** for **High-Speed**, **Full-Speed** and **Low-Speed**

In these modes, the maximum frequency of MCU is 208MHz, 104MHz and 26MHz, respectively, and the minimum V_{CORE} voltage requirement is 1.3V, 1.1V and 0.9V, respectively, for different performance requirements and low power optimization. The code can be executed from SRAM, PSRAM and Serial Flash device. There is also an independent clock gating control to lower the power consumption, if the peripherals are idle.

2) **Idle mode** for **Sleep**

In this mode, there is only 32kHz clock available, the other clock sources are turned off and the wakeup time to **LowSpeed** is only 7μs.

3) **PowerOff mode**

In this mode, all power supply sources are off except VRTC. It supports RTC timer to wake up the system and can detect the charger and if it's plugged-in, and more.

5.3. Power performance summary

Table 5.3-1 lists example current consumptions in VBAT domain. Note that the current measurement conditions are typical conditions for process, voltage and temperature. Besides, the current consumption in the table is based on the assumption that the power source for VCORE and BUCK are bucks with 85% efficiency and others are LDOs.

Table 5.3-1. Current consumption in different power modes

Power mode	Test Conditions	Typical	Unit
PowerOff	• System Off • No SRAM retained • Only RTC is alive	5.1	μA
Sleep	• 160kB SRAM is retained • Serial Flash in deep power down mode • All MTCMOS off • PSRAM power on	22.1	μA

(1) The data is retained in this mode.

(2) The wakeup time defines the instant the CPU can execute the first instruction.

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Power mode	Test Conditions	Typical	Unit
	• VCORE = 0.9V		

Bluetooth TX current	Bluetooth RF TX current, 0dBm	14.0	mA
Bluetooth RX current	Bluetooth RF RX current, 1 Mbps	6.0	mA
Bluetooth LE connection	1T1R; Period: 1280ms; TX Power: 0dBm; PSRAM on; Payload: Null	67.1	µA
Bluetooth LE advertising	3T3R; Period: 1280ms; TX Power: 0dBm; PSRAM on; Payload: 20 bytes	66.1	µA
Bluetooth paging scan	Period: 1280ms; Scan window: 11.25ms; PSRAM on;	131.1	µA
Bluetooth sniff	Period: 500ms; TX Power: 0dBm; Attempt: 4; PSRAM on;	83.1	µA
Bluetooth A2DP	• A2DP Stereo streaming MPEG-2,4 AAC LC: • 44.1kHz sampling • No sniff • Channel mode support: 2 • Audio headphone is disconnected • PSRAM power on	10.0	mA

5.4. Peripheral constraints and voltage for power mode

Table 5.4-1 and Table 5.4-2 list the operation state of peripherals in the always-on and power-down domains.

Table 5.4-1. Always-on power domain peripherals

Peripheral	High/Full/Low-speed Mode	Wakeup Source for Sleep and DeepSleep modes
eFUSE	Requirement: V_{CORE} = 1.2V	-
Always-on DMA controller	O	-
MIPI	Requirement: $V_{CORE} \geq 1.1V$	-
Keypad Scanner	O	O
GPC	O	O
GPT	O	O
PWM (0, 1)	O	-
Display PWM	O	-
ACCDET	O	O

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Table 5.4-2. INFRA_PD power-down domain peripherals

Module Description	High/Full/Low-speed Mode	Wakeup Source for Sleep and DeepSleep mode
Power-down DMA controller	O	-
TRNG	O	-
SDIO (0, 1)	O	O
Serial flash	O	-
PSRAM controller	O	-
UART (0, 1, 2, 3)	O	O
SPI_MASTER (0, 1, 2, 3)	O	-
SPI_SLAVE	O	O
PWM (2, 3, 4, 5)	O	-
I2C (0, 1, 2)	O	-
AUXADC	O	O
USB controller	requirement: $V_{CORE} \geq 1.2V$	O

- The wakeup source for peripherals, such as UART, is from IO. When an interrupt is detected, the sleep controller turns on the CPU_PD and INFRA_PD MTCMOS domains by default.
- There are voltage constraints for V_{CORE} for eFUSE, MIPI and USB. The voltage control is software configurable.

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6. Pin Description

6.1. MT2533D Ball Diagram

For MT2533D, a TFBGA 6.2mm*5.8mm, 172-ball, 0.4mm pitch package is offered. Pin-outs and the top view for this package are shown in Figure 6.1-1.

172	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	PPDM_DATAI1	PPDM_CLKO1	PTEST		DVDD_GPO	GPO_1		XTAL1	XTAL2	EXT_CLK_SEL	BT_LNA	AVDD13_BTRF		AVDD_VBT	GPIO_C1	A
B	PPDM_DATAI0	PPDM_CLKO0	PAVD	PSCL_H	PSDA_H	GPO_3	UTXD0	URXD0	FREF	AVSS_BT	AVSS_BT	DVDD_VIO_C	SCL0	SDA0	GPIO_C0	B
C		VDDIO	USB_VRT	VDDC	PRTC	SRCLKENAI	GND	AVDD18_DCXO	GND	AVSS_BT	AVSS_BT	GPIO_C4		CMRST		C
D	USB_DP	USB_DM	AVDD33_USB	AVSS33_USB	AVSS28_MIPI		GND	GND	AVSS_DCXO	AVSS_BT	GPIO_C3	GPIO_C2	CMCSD0	CMPDN	CMCSD1	D
E	CHG_DP	CHG_DM		PPDM_DATAO0	TDN		GND	GND	AVSS_BT		CMMCLK	CMCSK	DVDD_VSF	GPO_2	DVDD_VIO_A	E
F		PFRAME_TX	PPDM_CLKI	PPDM_DATAO1	TDP		GND	GND	GND	GND		GND		GPIO_A0		F
G	PFRAME_RX	PRX	PCLK_RX			AVDD28_MIPI	GND	GND	GND	GND	GPIO_A1	GPIO_A5	GPIO_A2	GPIO_A3	GPIO_B0	G
H		PIRQ	VDDK	TVRT	TCN		GND	GND	GND	GND	GPIO_B5	GPIO_A4		GPIO_B1	VDDK	H
J	PSDA	PSCL	PSPI_SS_	PSPI_MISO	TCP		AVDD_RTC	GND	GND	GND	GPIO_B2			LSCE_B		J
K	PSPI_MOSI	AVSS28_HP		PSPI_CLK		MCCK	DVDD33_VMC	GND	DVDD18_VSWXM		GPIO_B4	LPTE	GPIO_B3	LSA0	LSRSTB	K
L		AU_HPL	AU_HPR			PIO_RTC_VRF_EN	PIO_I2C_CLK	PIO_TESTMODE	RESETB_OUT	GPO_0	GND	LSDA		LSCK	AUXADCIN_3	L
M	AU_HSP	AU_HSN	AUD_VREF	AVSS_VREF	AVSS28_ABB	PIO_WDTRSTB_IN		PIO_VCORE_PREON	DVDD18_VIO18		MCDA1	AUXADCIN_1	AUXADCIN_4	AUXADCIN_2		M
N	AU_VIN0_N	AU_VIN1_P	AU_MICBIAS0	ACCDET	PIO_PMIC_INT	PIO_PSI0B	PIO_RESETB	PIO_PMU_PORSTB	PIO_DDLO_VRTC	PIO_RTC_ALARM	MCCM0	MCDA0	AUXADCIN_0	FSOURCE_D	DVDD_AUXADC	N
P	AU_VIN0_P	AU_VIN1_N		AVDD28_ABB	VIO18		PIO_PSI1B	PIO_I2C_DAT		MCDA3	MCDA2		XOUT	XIN	RTC_XOSC32_ENB	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 6.1-1. MT2533D ball diagram and top view

6.1.1. MT2533D pin coordination

Table 6.1-1. MT2533D pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	PPDM_DATAI1	C8	AVDD18_DCXO	F3	PPDM_CLKI
A2	PPDM_CLKO1	C9	GND	F4	PPDM_DATAO1

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Pin#	Net name	Pin#	Net name	Pin#	Net name
A3	PTEST	C10	AVSS_BT	F5	TDP
A5	DVDD_GPO	C11	AVSS_BT	F7	GND
A6	GPO_1	C12	GPIO_C4	F8	GND
A8	XTAL1	C14	CMRST	F9	GND
A9	XTAL2	D1	USB_DP	F10	GND
A10	EXT_CLK_SEL	D2	USB_DM	F12	GND
A11	BT_LNA	D3	AVDD33_USB	F14	GPIO_A0
A12	AVDD13_BTRF	D4	AVSS33_USB	G1	PFRAME_RX
A14	AVDD_VBT	D5	AVSS28_MIPI	G2	PRX
A15	GPIO_C1	D7	GND	G3	PCLK_RX
B1	PPDM_DATAI0	D8	GND	G6	AVDD28_MIPI
B2	PPDM_CLKO0	D9	AVSS_DCXO	G7	GND
B3	PAVD	D10	AVSS_BT	G8	GND
B4	PSCL_H	D11	GPIO_C3	G9	GND
B5	PSDA_H	D12	GPIO_C2	G10	GND
B6	GPO_3	D13	CMCSD0	G11	GPIO_A1
B7	UTXD0	D14	CMPDN	G12	GPIO_A5
B8	URXD0	D15	CMCSD1	G13	GPIO_A2
B9	FREF	E1	CHG_DP	G14	GPIO_A3
B10	AVSS_BT	E2	CHG_DM	G15	GPIO_B0
B11	AVSS_BT	E4	PPDM_DATAO0	H2	PIRQ
B12	DVDD_VIO_C	E5	TDN	H3	VDDK
B13	SCL0	E7	GND	H4	TVRT
B14	SDA0	E8	GND	H5	TCN
B15	GPIO_C0	E9	AVSS_BT	H7	GND
C2	VDDIO	E11	CMMCLK	H8	GND
C3	USB_VRT	E12	CMCSK	H9	GND
C4	VDDC	E13	DVDD_VSF	H10	GND
C5	PRTC	E14	GPO_2	H11	GPIO_B5
C6	SRCLKENAI	E15	DVDD_VIO_A	H12	GPIO_A4
C7	GND	F2	PFRAME_TX	H14	GPIO_B1
H15	VDDK	L6	PIO_RTC_VRF_EN	N6	PIO_PSI0B
J1	PSDA	L7	PIO_I2C_CLK	N7	PIO_RESETB
J2	PSCL	L8	PIO_TESTMODE	N8	PIO_PMU_PORSTB
J3	PSPI_SS_	L9	RESETB_OUT	N9	PIO_DDLO_VRTC
J4	PSPI_MISO	L10	GPO_0	N10	PIO_RTC_ALARM
J5	TCP	L11	GND	N11	MCCM0
J7	AVDD_RTC	L12	LSDA	N12	MCDA0
J8	GND	L14	LSCK	N13	AUXADCIN_0
J9	GND	L15	AUXADCIN_3	N14	FSOURCE_D
J10	GND	M1	AU_HSP	N15	DVDD_AUXADC
J11	GPIO_B2	M2	AU_HSN	P1	AU_VIN0_P
J14	LSCE_B	M3	AUD_VREF	P2	AU_VIN1_N
K1	PSPI_MOSI	M4	AVSS_VREF	P4	AVDD28_ABB

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Pin#	Net name	Pin#	Net name	Pin#	Net name
K2	AVSS28_HP	M5	AVSS28_ABB	P5	VIO18
K4	PSPI_CLK	M6	PIO_WDTRSTB_IN	P7	PIO_PSI1B
K6	MCCK	M8	PIO_VCORE_PREON	P8	PIO_I2C_DAT
K7	DVDD33_VMC	M9	DVDD18_VIO18	P10	MCDA3
K8	GND	M11	MCDA1	P11	MCDA2
K9	DVDD18_VSWXM	M12	AUXADCIN_1	P13	XOUT
K11	GPIO_B4	M13	AUXADCIN_4	P14	XIN
K12	LPTE	M14	AUXADCIN_2	P15	RTC_XOSC32_ENB
K13	GPIO_B3	N1	AU_VIN0_N		
K14	LSA0	N2	AU_VIN1_P		
K15	LSRSTB	N3	AU_MICBIAS0		
L2	AU_HPL	N4	ACCDET		
L3	AU_HPR	N5	PIO_PMIC_INT		

6.2. MT2533D series pins

Table 6.2-1 shows the acronym of each pin type and I/O structure. The functions and power domains of digital and analog pins are listed in Table 6.2-2 and Table 6.2-3, respectively.

Table 6.2-1. Acronym for pin types and I/O structure

Name	Abbreviation	Description
Pin Type	AI	Analog input
	AO	Analog output
	AIO	Analog bi-direction
	DI	Digital input
	DO	Digital output
	DIO	Digital bi-direction
	P	Power
	G	Ground
IO Structure	TYPE0	pull-up/down
	TYPE1	pull-up/down, 3.63V tolerance
	TYPE2	pull-up/down, Keypad scan (column) 3.63V tolerance
	TYPE3	pull-up/down, Keypad scan (row) 3.63V tolerance
	TYPE4	pull-up/down, AUXADC input, 3.63V tolerance

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Name	Abbreviation	Description
	TYPE5	Dedicated input I/O with weak pull-up resistor
	TYPE6	Dedicated input I/O with weak pull-down resistor
	TYPE7	No pull-up/down

Table 6.2-2. MT2533D digital pin function description and power domain

Pin Number	Pin Name	Pin Type	IO Structure	Pin Description	Alternate Pin Functions	Power domain
System						
L9	RESETB_OUT	DIO	TYPE1	System reset output	-	DVDD18_VIO18
C6	SRCLKENAI	DIO	TYPE1	26MHz clock request by external devices	-	DVDD_GPO
N5	PIO_PMIC_INT	DIO	TYPE5	Interrupt from PMIC	-	VIO18
N7	PIO_RESETB	DIO	TYPE7	System reset in	-	VIO18
N6	PIO_PSI0B	DIO	TYPE7	Special power control signal to PMIC	-	VIO18
P7	PIO_PSI1B	DIO	TYPE7	Special power control signal to PMIC	-	VIO18
P8	PIO_I2C_DAT	DIO	TYPE0	I2C data pin	-	VIO18
L7	PIO_I2C_CLK	DIO	TYPE0	I2C clock pin	-	VIO18
M6	PIO_WDTRSTB_IN	DIO	TYPE7	Watchdog reset output	-	VIO18
N8	PIO_PMU_PORSTB	DIO	TYPE7	RTC reset	-	AVDD_RTC
L6	PIO_RTC_VRF_EN	DIO	TYPE7	Control PMIC for 32K-less application	-	AVDD_RTC
M8	PIO_VCORE_PREON	DIO	TYPE7	Internal power sequence control	-	AVDD_RTC
N9	PIO_DDLO_VRTC	DIO	TYPE7	PMIC assert DDLO for 32K-less application	-	AVDD_RTC
L8	PIO_TESTMODE	DIO	TYPE7	Test mode input	-	AVDD_RTC
N10	PIO_RTC_ALARM	DIO	TYPE7	Wakeup PMIC for 32K-less application	-	AVDD_RTC
General purpose I/O – Group A						
F14	GPIO_A0	DIO	TYPE1	GPIO, Group A, Pin 0	SDIO (1), I2S Slave,	DVDD_VIO_A

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Pin Number	Pin Name	Pin Type	IO Structure	Pin Description	Alternate Pin Functions	Power domain
					UART (1), SPI_MASTER (0)	
G11	GPIO_A1	DIO	TYPE1	GPIO, Group A, Pin 1	SDIO (1), I2S Slave, UART (1), SPI_MASTER (0)	DVDD_VIO_A
G13	GPIO_A2	DIO	TYPE1	GPIO, Group A, Pin 2	SDIO (1), I2S Slave, UART (2), SPI_MASTER (0)	DVDD_VIO_A
G14	GPIO_A3	DIO	TYPE1	GPIO, Group A, Pin 3	SDIO (1), I2S Slave, UART (2), SPI_MASTER (0)	DVDD_VIO_A
H12	GPIO_A4	DIO	TYPE1	GPIO, Group A, Pin 4	SDIO (1), I2C (2)	DVDD_VIO_A
G12	GPIO_A5	DIO	TYPE1	GPIO, Group A, Pin 5	SDIO (1), I2C (2)	DVDD_VIO_A
General purpose I/O – Group B						
G15	GPIO_B0	DIO	TYPE3	GPIO, Group B, Pin 0, with KEYPAD function	Keypad Scanner, UART (1,3), CM4 JTAG	DVDD_VIO_C
H14	GPIO_B1	DIO	TYPE3	GPIO, Group B, Pin 1, with KEYPAD function	Keypad Scanner, I2C (2), CM4 JTAG	DVDD_VIO_C
J11	GPIO_B2	DIO	TYPE3	GPIO, Group B, Pin 2, with KEYPAD function	Keypad Scanner, I2C (2)	DVDD_VIO_C
K13	GPIO_B3	DIO	TYPE2	GPIO, Group B, Pin 3, with KEYPAD function	Keypad Scanner, GPCOUNTER (0), CM4 JTAG	DVDD_VIO_C
K11	GPIO_B4	DIO	TYPE2	GPIO, Group B, Pin 4, with KEYPAD function	Keypad Scanner, UART (1,3), CM4 JTAG	DVDD_VIO_C
H11	GPIO_B5	DIO	TYPE2	GPIO, Group B, Pin 5, with KEYPAD function	Keypad Scanner, CM4 JTAG	DVDD_VIO_C
General purpose I/O – Group C						
B15	GPIO_C0	DIO	TYPE1	GPIO, Group C, Pin 0	I2S Master, I2S Slave, PWM (0), SPI_MASTER (1)	DVDD_VIO_C
A15	GPIO_C1	DIO	TYPE1	GPIO, Group C, Pin 1	I2S Master,	DVDD_VIO_C

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Pin Number	Pin Name	Pin Type	IO Structure	Pin Description	Alternate Pin Functions	Power domain
					I2S Slave, PWM (1), SPI_MASTER (1)	
D12	GPIO_C2	DIO	TYPE1	GPIO, Group C, Pin 2	I2S Master, I2S Slave, PWM (2), SPI_MASTER (1)	DVDD_VIO_C
D11	GPIO_C3	DIO	TYPE1	GPIO, Group C, Pin 3	I2S Master, I2S Slave, PWM (3), SPI_MASTER (1)	DVDD_VIO_C
C12	GPIO_C4	DIO	TYPE1	GPIO, Group C, Pin 4	PWM (4)	DVDD_VIO_C
General purpose I/O with AUXADC input channel						
N13	AUXADCIN_0	DIO	TYPE4	GPIO with AUXADX input channel 0	AUXADCIN (0), UART (2), PWM (0), SPI_MASTER (0,1), I2S Master	DVDD_AUXADC
M12	AUXADCIN_1	DIO	TYPE4	GPIO with AUXADX input channel 1	AUXADCIN (1), UART (2), PWM (1), SPI_MASTER (0,1), I2S Master	DVDD_AUXADC
M14	AUXADCIN_2	DIO	TYPE4	GPIO with AUXADX input channel 2	AUXADCIN (2), UART (3), SPI_MASTER (0,1), I2S Master	DVDD_AUXADC
L15	AUXADCIN_3	DIO	TYPE4	GPIO with AUXADX input channel 3	AUXADCIN (3), UART (3), SPI_MASTER (0,1), I2S Master	DVDD_AUXADC
M13	AUXADCIN_4	DIO	TYPE4	GPIO with AUXADX input channel 4	AUXADCIN (4)	DVDD_AUXADC
General purpose output						
L10	GPO_0	DO	TYPE1	General purpose output, Pin 0	Display PWM	DVDD18_VIO18
A6	GPO_1	DO	TYPE1	General purpose output, Pin 1	-	DVDD_GPO

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Pin Number	Pin Name	Pin Type	IO Structure	Pin Description	Alternate Pin Functions	Power domain
E14	GPO_2	DO	TYPE1	General purpose output, Pin 2	-	DVDD_VIO_A
B6	GPO_3	DO	TYPE1	General purpose output, Pin 3	-	DVDD_GPO
UART interface						
B8	URXD0	DIO	TYPE1	UART0 receive data	-	DVDD_GPO
B7	UTXD0	DIO	TYPE1	UART0 transmit data	-	DVDD_GPO
Camera interface						
C14	CMRST	DIO	TYPE1	CMOS sensor reset signal output	GPCOUNTER (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
D14	CMPDN	DIO	TYPE1	CMOS sensor power down control	PCM, SPI_MASTER (2,3), SPI_SLAVE (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
D13	CMCSD0	DIO	TYPE1	CMOS sensor data input 0	PCM, SPI_MASTER (2,3), SPI_SLAVE (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
D15	CMCSD1	DIO	TYPE1	CMOS sensor data input 1	PCM, SPI_MASTER (2,3), SPI_SLAVE (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
E11	CMMCLK	DIO	TYPE1	CMOS sensor pixel clock input	PCM, SPI_MASTER (2,3), SPI_SLAVE (0), Cortex-M4 JTAG, SDIO (1)	DVDD_VIO_A
E12	CMCSK	DIO	TYPE1	CMOS sensor pixel clock output	SDIO (1)	DVDD_VIO_A
SDIO interface						
K6	MCCK	DIO	TYPE1	SD serial clock/memory stick serial clock	I2C (0,2), PWM (0), UART (1), SDIO (0)	DVDD33_VMC

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Pin Number	Pin Name	Pin Type	IO Structure	Pin Description	Alternate Pin Functions	Power domain
N11	MCCM0	DIO	TYPE1	SD command output/memory stick bus state output	I2C (0,2), PWM (1), UART (1), SDIO (0)	DVDD33_VMC
N12	MCDA0	DIO	TYPE1	SD serial data IO 0/memory stick serial data IO	SPI_MASTER (3), SPI_SLAVE (0), PWM (2), PCM, SDIO (1)	DVDD33_VMC
M11	MCDA1	DIO	TYPE1	SD serial data IO 1/memory stick serial data IO	SPI_MASTER (3), SPI_SLAVE (0), PWM (2), PCM, SDIO (1)	DVDD33_VMC
P11	MCDA2	DIO	TYPE1	SD serial data IO 2/memory stick serial data IO	SPI_MASTER (3), SPI_SLAVE (0), PWM (2), PCM, SDIO (1)	DVDD33_VMC
P10	MCDA3	DIO	TYPE1	SD serial data IO 3/memory stick serial data IO	SPI_MASTER (3), SPI_SLAVE (0), PWM (2), PCM, SDIO (1)	DVDD33_VMC
I2C interface						
B13	SCL0	DIO	TYPE1	I2C clock pin of controller 0	-	DVDD_VIO_A
B14	SDA0	DIO	TYPE1	I2C data pin of controller 0	-	DVDD_VIO_A
LCM interface						
K15	LSRSTB	DIO	TYPE1	Serial display interface reset signal	I2C (1)	DVDD18_VIO18
J14	LSCE_B	DIO	TYPE1	Serial display interface chip select output	I2C (1), SPI_MASTER (2)	DVDD18_VIO18
L14	LSCK	DIO	TYPE1	Serial display interface clock	SPI_MASTER (2)	DVDD18_VIO18
L12	LSDA	DIO	TYPE1	Serial display interface data	I2C (1), SPI_MASTER (2)	DVDD18_VIO18
K14	LSA0	DIO	TYPE1	Serial display interface address	SPI_MASTER (2)	DVDD18_VIO18
K12	LPTE	DIO	TYPE1	Serial display tearing signal	I2C (1)	DVDD18_VIO18

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Table 6.2-3 MT2533D analog pin function description and power domain

Pin Number	Pin Name	Pin Type	Pin Description	Power domain
Bluetooth				
A11	BT_LNA	AIO	Bluetooth RF single-ended input	AVDD_VBT
Clock 26MHz DCXO				
B9	FREF	AO	DCXO reference clock output	AVDD18_DCXO
A8	XTAL1	AIO	Input 1 for DCXO crystal	AVDD18_DCXO
A9	XTAL2	AIO	Input 2 for DCXO crystal	AVDD18_DCXO
A10	EXT_CLK_SEL	AIO	DCXO mode selection	AVDD18_DCXO
USB				
D2	USB_DM	AIO	D- data input/output	-
D1	USB_DP	AIO	D+ data input/output	-
C3	USB_VRT	AIO	USB reference voltage	-
Real-time clock				
P14	XIN	AIO	Input pin for 32kHz crystal	AVDD_RTC
P13	XOUT	AIO	Input pin for 32kHz crystal	AVDD_RTC
P15	RTC_XOSC32_ENB	DIO	Pin option for external 32K crystal	AVDD_RTC
Analog baseband				
L3	AU_HPR	AO	Audio head phone output (R channel)	AVDD28_ABB
L2	AU_HPL	AO	Audio head phone output (L channel)	AVDD28_ABB
M1	AU_HSP	AO	Voice handset output (positive)	AVDD28_ABB
M2	AU_HSN	AO	Voice handset output (negative)	AVDD28_ABB
P1	AU_VIN0_P	AI	Microphone 0 input (positive)	AVDD28_ABB
N1	AU_VIN0_N	AI	Microphone 0 input (negative)	AVDD28_ABB
N2	AU_VIN1_P	AI	Microphone 1 input (positive)	AVDD28_ABB
P2	AU_VIN1_N	AI	Microphone 1 input (negative)	AVDD28_ABB
M3	AUD_VREF	AI	Audio reference voltage	-
M4	AVSS_VREF	AI	Audio reference ground	-
N3	AU_MICBIAS0	AI	Microphone bias source 0	-
N4	ACCDET	AI	Accessory detection	AVDD28_ABB
Analog power				
D3	AVDD33_USB	P	USB 3.3V power input	VDDIO
G6	AVDD28_MIPI	P	MIPI 2.8V power input	VDDIO
P4	AVDD28_ABB	P	ABB 2.8V power input	VDDIO
-	AVDD_BT	P	BTRF power input	VDDIO
A12	AVDD13_BTRF	P	BTRF 1.3V power input	VDDIO

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Pin Number	Pin Name	Pin Type	Pin Description	Power domain
C8	AVDD18_DCXO	P	DCXO 1.8V power input	VDDIO
J7	AVDD_RTC	P	RTC power input	VDDIO
Analog ground				
D4	AVSS33_USB	G	USB ground	VDDIO
D5	AVSS28_MIPI	G	MIPI ground	VDDIO
M5	AVSS28_ABB	G	ABB ground	VDDIO
K2	AVSS28_HP	G	ABB headphone ground	VDDIO
B10 B11 C10 C11 D10 E9	AVSS_BT	G	BT ground	VDDIO
D9	AVSS_DCXO	G	DCXO ground	VDDIO
Digital IO power				
E15	DVDD_VIO_A	P	Power input of GPIO group A	-
B12	DVDD_VIO_C	P	Power input of GPIO group C	-
N15	DVDD_AUXADC	P	Power input of AUXADC	-
A5	DVDD_GPO	P	Power input of GPO group	-
M9	DVDD18_VIO18	P	Power input of LCM and VIO18 IO	-
K7	DVDD33_VMC	P	Power input of MSDC IO	-
E13	DVDD_VSF	P	Power input of serial flash IO	-
K9	DVDD18_VSWXM	P	Power input of SIP PSRAM	-
C2	VDDIO	P	Power input of DSP	-
C4	VDDC	P	DSP Core monitor	-
Digital core power				
H13 H15	VDDK	P	Core power	-
eFUSE power				
N14	FSOURCE_D	P	EFUSE power input of digital	-
Digital ground				
C7 C9 D7 D8 E7 E8 F7 F8 F9 F10 F12 G7 G8 G9 G10 H7 H8 H9 H10 J8 J9 J10 K8 L11	GND	G	Ground	-
DSP interface				
B1	PPDM_DATAI0	DIO	PDM data from MIC0 and MIC1	VDDIO
A1	PPDM_DATAI1	DIO	PDM data from MIC2 and MIC3.	VDDIO
B2	PPDM_CLKO0	DIO	PDM clock output to microphone	VDDIO
A2	PPDM_CLKO1	DIO	2nd PDM clock to microphone	VDDIO
A3	PTEST	DIO	DSP Test pin	VDDIO

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Pin Number	Pin Name	Pin Type	Pin Description	Power domain
B3	PAVD	DIO	AVD input from digital microphone	VDDIO
B4	PSCL_H	DIO	I2C clock to digital microphone	VDDIO
B5	PSDA_H	DIO	I2C clock to digital microphone	VDDIO
C5	PRTC	DIO	Clock input as reference in power saving mode	VDDIO
K4	PSPI_CLK	DIO	DSP SPI clock	VDDIO
J4	PSPI_MISO	DIO	Data from DSP SPI slave to SPI master	VDDIO
K1	PSPI_MOSI	DIO	Data from SPI master to DSP SPI slave	VDDIO
J3	PSPI_SS_	DIO	DSP SPI chip select	VDDIO
H2	PIRQ	DIO	DSP Wake-up trigger	VDDIO
J1	PSDA	DIO	DSP I2C data	VDDIO
J2	PSCL	DIO	DSP I2C clock	VDDIO
G1	PFRAME_RX	DIO	Frame of RX of I2S	VDDIO
G3	PCLK_RX	DIO	BCLK of RX of I2S	VDDIO
G2	PRX	DIO	RX of I2S	VDDIO
F2	PFRAME_TX	DIO	Frame of TX	VDDIO
F3	PPDM_CLKI	DIO	PDM clock from CODEC or BCLK of I2S	VDDIO
F4	PPDM_DATAO1	DIO	MIC2 and MIC3 to CODEC	VDDIO
E4	PPDM_DATAO0	DIO	MIC0 and MIC1 to CODEC	VDDIO

6.3. MT2533D pin multiplexing

MT2533D platform offers 48 GPIO pins. By setting up the control registers, the MCU software can control the direction, the output value and read the input values on the pins. The GPIOs and GPOs are multiplexed with other functions to reduce the pin count. The clock can be configured by software to feed external devices with different frequencies. There are six clock-out ports embedded in 48 GPIO pins and each clock-out can be programmed to output an appropriate clock source. In addition, when two GPIOs function for the same peripheral IP, the smaller GPIO serial number has higher priority over the bigger one.

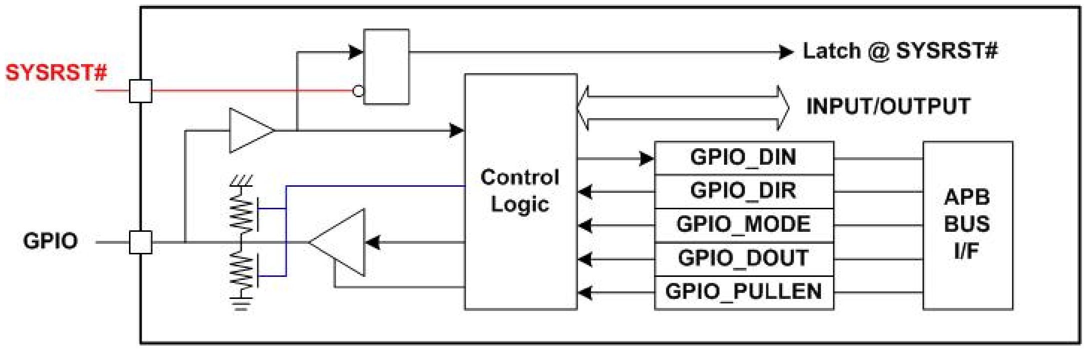

Figure 6.3-1. GPIO block diagram

MT2533D has rich peripheral functions with corresponding peripheral signals, as shown below. The SDIO, SPI Master and SPI Slave can support signal groups allocated on different pins.

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Alternate Function	Signal List
SDIO (0)	MC0_CK
	MC0_CM0
	MC0_DA0
	MC0_DA1
	MC0_DA2
	MC0_DA3
SDIO (1)	MC1_A_CK
	MC1_A_CM0
	MC1_A_DA0
	MC1_A_DA1
	MC1_A_DA2
	MC1_A_DA3
	MC1_B_DA3
	MC1_B_DA2
	MC1_B_CM0
	MC1_B_CK
	MC1_B_DA0
	MC1_B_DA1

Alternate Function	Signal List
UART (0)	URXD0
	UTXD0
UART (1)	URXD1
	UTXD1
UART (2)	URXD2
	UTXD2
UART (3)	URXD3
	UTXD3
I2C (0)	SCL0
	SDA0
I2C (1)	SCL1
	SDA1
I2C (2)	SCL2
	SDA2
I2S Master	MA_EDIDO
	MA_EDIDI
	MA_EDIWS
	MA_EDICK

Alternate Function	Signal List
SPI_MASTER (0)	MA_SPI0_A_CS
	MA_SPI0_A_SCK
	MA_SPI0_A_MOSI
	MA_SPI0_A_MISO
	MA_SPI0_B_CS
	MA_SPI0_B_SCK
	MA_SPI0_B_MOSI
	MA_SPI0_B_MISO
SPI_MASTER (1)	MA_SPI1_A_CS
	MA_SPI1_A_SCK
	MA_SPI1_A_MOSI
	MA_SPI1_A_MISO
	MA_SPI1_B_CS
	MA_SPI1_B_SCK
	MA_SPI1_B_MOSI
	MA_SPI1_B_MISO
SPI_MASTER (2)	MA_SPI2_A_CS
	MA_SPI2_A_SCK
	MA_SPI2_A_MOSI
	MA_SPI2_A_MISO

Alternate Function	Signal List
I2S Slave	SLA_EDIDO
	SLA_EDIDI
	SLA_EDIWS
	SLA_EDICK
PWM (0)	PWM0
PWM (1)	PWM1
PWM (2)	PWM2
PWM (3)	PWM3
PWM (4)	PWM4
PWM (5)	PWM5
Camera Interface	CMRST
	CMPDN
	CMCSD0
	CMCSD1
	CMMCLK
	CMCSK
LCM Interface	LSRSTB
	LSCE_B
	LSCK
	LSDA

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SPI_MASTER (3)	MA_SPI3_A_CS MA_SPI3_A_SCK MA_SPI3_A_MOSI MA_SPI3_A_MISO
	MA_SPI3_B_CS MA_SPI3_B_SCK MA_SPI3_B_MOSI MA_SPI3_B_MISO
SPI_SLAVE (0)	SLV_SPI0_CS SLV_SPI0_SCK SLV_SPI0_MOSI SLV_SPI0_MISO
PCM	DAISYNC DAIPCMIN DAICLK DAIPCMOUT

	LSA0 LPTE
AUXADC	AUXADCIN_0 AUXADCIN_1 AUXADCIN_2 AUXADCIN_3 AUXADCIN_4
CM4 JTAG	JTDI JTMS JTCK JTRSTB JTDO

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Table 6.3-1. PinMux description

Pin Name	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6	Mode 7	Mode 8	Mode 9
General purpose I/O – Group A										
GPIO_A0	GPIO4	EINT3	MC1_A_CK	SLA_EDIDO			URXD1	MA_SPI0_B_CS		
GPIO_A1	GPIO5	EINT4	MC1_A_CM0	SLA_EDIDI			UTXD1	MA_SPI0_B_SCK		
GPIO_A2	GPIO6	EINT5	MC1_A_DA0	SLA_EDIWS	URXD2			MA_SPI0_B_MOSI		
GPIO_A3	GPIO7	EINT6	MC1_A_DA1	SLA_EDICK	UTXD2		BT_BUCK_EN_HW	MA_SPI0_B_MISO		
GPIO_A4	GPIO8	EINT7	MC1_A_DA2				SCL2			
GPIO_A5	GPIO9	EINT8	MC1_A_DA3				SDA2			
General purpose I/O – Group B										
GPIO_B0	GPIO18	KCOL2	URXD1	URXD3			LSCE1_B1		JTDI	BTJTDI
GPIO_B1	GPIO19	KCOL1	EINT18	UART0_RTS	SCL2				JTMS	BTJTMS
GPIO_B2	GPIO20	KCOL0	GPSFSYNC	UART0_CTS	SDA2		MA_SPI2_CS1			
GPIO_B3	GPIO21	KROW2		GPCOUNTER_0	UART1_RTS (Out)				JTCK	BTJTCK
GPIO_B4	GPIO22	KROW1	UTXD1	UTXD3					JTDO	BTDBGIN
GPIO_B5	GPIO23	KROW0	EINT19	CLKO0	UART1_CTS (In)		MC_RST		JTRSTB	BTJTRSTB
General purpose I/O – Group C										
GPIO_C0	GPIO11	EINT9	BT_BUCK_EN_HW	MA_EDIDO	MA_SPI1_B_CS	PWM0	SLA_EDIDO			
GPIO_C1	GPIO12	EINT10		MA_EDIDI	MA_SPI1_B_SCK	PWM1	SLA_EDIDI			
GPIO_C2	GPIO13	EINT11	CLKO3	MA_EDIWS	MA_SPI1_B_MOSI	PWM2	SLA_EDIWS			
GPIO_C3	GPIO14	EINT12	CLKO4	MA_EDICK	MA_SPI1_B_MISO	PWM3	SLA_EDICK			
GPIO_C4	GPIO15	EINT13				PWM4				

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General purpose I/O with AUXADC input channel										
AUXADCIN_0	GPIO0	EINT0	AUXADCIN_0	URXD2	PWM0	MA_SPI1_A_CS	MA_EDIDO	MA_SPI0_A_CS		BTJTDO
AUXADCIN_1	GPIO1	EINT1	AUXADCIN_1	UTXD2	PWM1	MA_SPI1_A_SCK	MA_EDIDI	MA_SPI0_A_SCK		BTDBGACKN
AUXADCIN_2	GPIO2	EINT2	AUXADCIN_2	URXD3	UART0_CTS (In)	MA_SPI1_A_MOSI	MA_EDIWS	MA_SPI0_A_MOSI		BT_BUCK_EN_HW
AUXADCIN_3	GPIO3	EINT14	AUXADCIN_3	UTXD3	UART0_RTS (Out)	MA_SPI1_A_MISO	MA_EDICK	MA_SPI0_A_MISO		BT_PRI
AUXADCIN_4	GPIO10	EINT15	AUXADCIN_4							BT_PRI
General purpose output										
GPO_0	GPO44	LSCE1_B1	DISP_PWM							
GPO_1	GPO46	MA_SPI0_CS1								
GPO_2	GPO47	MA_SPI1_CS1								
GPO_3	GPO48	MA_SPI3_CS1								
UART Interface										
URXD0	GPIO16	URXD0		EINT16						
UTXD0	GPIO17	UTXD0		EINT17						
Camera Interface										
CMRST	GPIO24	CMRST	LSRSTB	CLKO1	EINT9	GPCOUNTER_0	JTDI		MC1_B_DA3	
CMPDN	GPIO25	CMPDN	LSCK1	DAICLK	MA_SPI2_A_CS	MA_SPI3_A_CS	JTMS		MC1_B_DA2	SLV_SPI0_CS
CMCSD0	GPIO26	CMCSD0	LSCE_B1	DAIPCMIN	MA_SPI2_A_SCK	MA_SPI3_A_SCK	JTCK		MC1_B_CM0	SLV_SPI0_SCK
CMCSD1	GPIO27	CMCSD1	LSDA1	DAIPCMOUT	MA_SPI2_A_MOSI	MA_SPI3_A_MOSI	JTRSTB		MC1_B_CK	SLV_SPI0_MOSI
CMMCLK	GPIO28	CMMCLK	LSA0DA1	DAISYNC	MA_SPI2_A_MISO	MA_SPI3_A_MISO	JTDO		MC1_B_DA0	SLV_SPI0_MISO
CMCSK	GPIO29	CMCSK	LPTE		CMCSD2	EINT10			MC1_B_DA1	
SDIO Interface										
MCCK	GPIO30	SCL0	EINT11	PWM0	URXD1	MC0_CK				SCL2
MCCM0	GPIO31	SDA0	EINT12	PWM1	UTXD1	MC0_CM0				SDA2

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MCDA0	GPIO32	SLV_SPI0_CS	EINT13	PWM2	DAISYNC	MC0_DA0				MA_SPI3_B_CS
MCDA1	GPIO33	SLV_SPI0_SCK	EINT14	PWM3	DAIPCMIN	MC0_DA1				MA_SPI3_B_SCK
MCDA2	GPIO34	SLV_SPI0_MOSI	EINT15	PWM4	DAICLK	MC0_DA2				MA_SPI3_B_MOSI
MCDA3	GPIO35	SLV_SPI0_MISO	EINT3	PWM5	DAIPCMOUT	MC0_DA3	CLKO2			MA_SPI3_B_MISO
I2C Interface										
SCL0	GPIO36	SCL0	SCL1							
SDA0	GPIO37	SDA0	SDA1							
LCM Interface										
LSRSTB	GPIO38	LSRSTB		CMRST	CLKO3					SCL1
LSCE_B	GPIO39	LSCE_B0	EINT4	CMCSD0	CLKO4				SCL1	MA_SPI2_C_CS
LSCK	GPIO40	LSCK0		CMPDN						MA_SPI2_C_SCK
LSDA	GPIO41	LSDA0	EINT5	CMCSD1	WIFITOBT				SDA1	MA_SPI2_C_MOSI
LSA0	GPIO42	LSA0DA0	LSCE1_B0	CMMCLK					CLKO5	MA_SPI2_C_MISO
LPTE	GPIO43	LPTE	EINT6	CMCSK	CMCSD2					SDA1

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7. System Configuration

7.1. System mode selection and trapping

Apply the following pin trappings to configure the chip in different modes (see Table 7.1-1)

Table 7.1-1. Mode selection

Mode Selection	Pin name	Description	Trapping Resistor	Trapping condition
26MHz clock source	EXT_CLK_SEL	GND: Uses DCXO as 26MHz clock source AVDD18_DCXO: Uses external clock as 26M clock source	Pull-down/up with 10kΩ resistor	DCXO Power-on reset
Serial flash power supply voltage	GPO_3	GND: Uses 1.8V serial flash device DVDD_GPO: Uses 3.3V serial flash device	Pull-down with 10kΩ resistor (Default internal pull-down with 47kΩ resister)	Power-on reset
USB download	GPIO_B2	GND: Boots ROM to enter USB download mode DVDD_VIO_C: Normal boot-up mode	Pull-down with 10K resistor (Default internal pull-down with 47kΩ resister)	Power-on reset
Cortex-M4 JTAG pin out	{GPO_1,GPO_0}	{GND, GND}: No JTAG {GND, DVDD18_VIO18}: JTAG at keypad pins { DVDD_GPO, GND}: JTAG at GPIO pins { DVDD_GPO, DVDD18_VIO18}: JTAG at camera pins	Pull-up with 10K resistor (Default internal pull-down with 47kΩ resistor)	Power-on reset

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8. Electrical Characteristics

8.1. Absolute maximum ratings

Table 8.1-1. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
VDDK	1.3v core power	-0.3	+1.43	V

Table 8.1-2. Absolute maximum ratings for I/O power supply

Symbol or pin name	Description	Min.	Typ.1	Typ.2	Max.	Unit
DVDD_VIO_A	Power supply for GPIO group A	1.62	1.8	2.8	3.08	V
DVDD_VIO_C	Power supply for GPIO group C	1.62	1.8	2.8	3.08	V
DVDD_AUXADC	Power supply for AUXADC	2.52	-	2.8	3.08	V
DVDD_GPO	Power supply for GPO group	1.62	1.8	2.8	3.08	V
DVDD18_VIO18	Power supply for IO 1.8V group	1.62	1.8	-	1.98	V
DVDD33_VMC	Power supply for SDIO group	1.62	1.8	3.3	3.63	V

Table 8.1-3. Absolute maximum ratings for voltage input

Symbol or pin name	Description	Min.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	3.63	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.63	V

Table 8.1-4. Absolute maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	°C

8.2. Operating conditions

8.2.1. General operating conditions

Table 8.2-1. General operating conditions

Item	Description	Condition	Min.	Typ.	Max.	Unit
F_{CPU}	Internal Cortex-M4 & TCM & Cache clock	V_{CORE} = 0.9V	0	-	26	MHz
		V_{CORE} = 1.1V	0	-	104	MHz
		V_{CORE} = 1.3V	0	-	208	MHz
F_{MEMS}	Internal memory (SFC and EMI) related AHB and APB clock.	V_{CORE} = 0.9V	0	-	13	MHz
		V_{CORE} = 1.1V	0	-	52	MHz

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Item	Description	Condition	Min.	Typ.	Max.	Unit
	Synchronous with F_{CPU}.	V_{CORE} = 1.3V	0	-	104	MHz
F_{PERI}	Internal peripheral AHB and APB clock. Asynchronous with FCPU.	V_{CORE} = 0.9V	0	-	13	MHz
		V_{CORE} = 1.1V to 1.3V	0	-	62.4	MHz

Table 8.2-2. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VDDK	Digital core power	0.7	1.2	1.3	V

Table 8.2-3. Recommended operating conditions for voltage input

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V

Table 8.2-4. Recommended operating conditions for operating temperature

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
Tc	Operating temperature	-20	-	85	°C

8.2.2. Input or output port characteristics

Table 8.2-5. Electrical characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH1	Digital high input current for IO Type 1	• PU/PD disabled, • DVDIO = 2.8V, • 2.1 < VIN1 < 3.1	-5	-	5	µA
		• PU enabled, • DVDIO = 2.8V, • 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		• PD enabled, • DVDIO = 2.8V, • 2.1<VIN1<3.1	6.1	-	82.5	
DIIL1	Digital low input current for IO Type 1	• PU/PD disabled, • DVDIO = 2.8V, • -0.3 < VIN1 < 0.7	-5	-	5	µA
		• PU enabled, • DVDIO = 2.8V, • -0.3 < VIN1 < 0.7	-82.5	-	-6.1	
		• PD enabled, • DVDIO = 2.8V,	-12.5	-	22.5	

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• -0.3 < VIN1 < 0.7				
DIOH1	Digital high output current for IO Type 1	• DVOH > 2.38V, • DVDIO = 2.8V	-16	-	-	mA
DIOL1	Digital low output current for IO Type 1	• DVOL < 0.42V, • DVDIO = 2.8V	-	-	16	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	• DVDIO = 2.8V	40	85	190	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	• DVDIO = 2.8V	40	85	190	kΩ
DVOH1	Digital output high voltage for IO Type 1	• DVDIO = 2.8V	2.38			V
DVOL1	Digital output low voltage for IO Type 1	• DVDIO = 2.8V			0.42	V
DIIH2	Digital high input current for IO Type 2	• PU/PD disabled, • DVDIO = 2.8V, • 2.1 < VIN1 < 3.1	-5	-	5	µA
		• PU enabled, • DVDIO = 2.8V, • 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		• PD enabled, • DVDIO = 2.8V, • 2.1<VIN1<3.1	6.1	-	82.5	
		• PU/PD disabled, • DVDIO = 1.8V, • 1.35 < VIN1 < 2.1	-5	-	5	µA
		• PU enabled, • DVDIO = 1.8V, • 1.35 < VIN1 < 2.1	-11.4	-	9.3	
		• PD enabled, • DVDIO = 1.8V, • 1.35 < VIN1 < 2.1	-0.8	-	35	
DIIL2	Digital low input current for IO Type 2	• PU/PD disabled, • DVDIO = 2.8V, • -0.3 < VIN2 < 0.7	-5	-	5	µA
		• PU enabled, • DVDIO = 2.8V, • -0.3 < VIN2 < 0.7	-82.5	-	-6.1	
		• PD enabled, • DVDIO = 2.8V, • -0.3 < VIN2 < 0.7	-12.5	-	22.5	

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Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		• PU/PD disabled, • DVDIO = 1.8V, • -0.3 < VIN1 < 0.45	-5	-	5	µA
		• PU enabled, • DVDIO = 1.8V, • -0.3 < VIN1 < 0.45	-35	-	0.8	
		• PD enabled, • DVDIO = 1.8V, • -0.3 < VIN1 < 0.45	-9.3	-	11.4	
DIOH2	Digital high output current for IO Type 2	• DVOH > 2.38V, • DVDIO = 2.8V	-16	-	-	mA
		• DVOH > 1.53V, • DVDIO = 1.8V	-12	-	-	mA
DIOL2	Digital low output current for IO Type 2	• DVOL < 0.42V, • DVDIO = 2.8V	-	-	16	mA
		• DVOL < 0.27V, • DVDIO = 1.8V	-	-	12	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	• DVDIO = 2.8V	40	85	190	kΩ
		• DVDIO = 1.8V	70	150	320	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	• DVDIO = 2.8V	40	85	190	kΩ
		• DVDIO = 1.8V	70	150	320	kΩ
DVOH2	Digital output high voltage for IO Type 2	• DVDIO = 2.8V	2.38			V
		• DVDIO = 1.8V	1.53			V
DVOL2	Digital output low voltage for IO Type 2	• DVDIO = 2.8V			0.42	V
		• DVDIO = 1.8V			0.27	V

8.2.3. External clock source

8.2.3.1. Digitally Controlled Crystal Oscillator (DCXO)

The Digitally Controlled Crystal Oscillator (DCXO) uses a two-pin 26MHz crystal resonator. Both crystals with 1612 and 3225 footprint are supported. See Table 8.2-6 for the supported ranges of the crystal resonator capacitance load and tuning sensitivity. On-chip programmable capacitor array is used for frequency tuning, whereby the tuning range is ±50ppm. This DCXO supports 32.768kHz crystal-less operation.

Table 8.2-6. DCXO Characteristics (TA = 250C, VDD = 1.8V unless otherwise stated) (1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating frequency	Fref			26		MHz
Crystal C load	CL		7	7.5		pF
Crystal tuning	TS		10	33		ppm/pF

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
sensitivity						
Static range	SR	CDAC from 0 to 511	± 40	± 50		ppm
Start-up time	TDCXO	Frequency error < 10ppm Amplitude > 90 %		0.6	2.5	ms
Pushing figure				0.2		ppm/V
Fref buffer output level	VFref	Max. loading = 10pF		1.1		V_{p-p}
Fref buffer output phase noise		10kHz offset jitter noise		-140		dBc/Hz

(1) Guaranteed by design, not tested in production.

8.2.3.2. 32.768kHz crystal oscillator (XOSC32)

The low-power 32.768kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. It is designed to be a clock source of RTC for lower power platform. See Table 8.2-7 for the key performance.

The crystal parameters determine the oscillation allowance. Table 8.2-8 lists recommendations for the crystal parameters to be used well with XOSC32.

Table 8.2-7. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power		1.8		V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	35	50		%
	Current consumption			1.5	µA
T	Operating temperature	-40		85	°C

Table 8.2-8. Recommended parameters for 32.768kHz crystal oscillator

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level			1.5	µW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	kΩ
C0	Static capacitance		1.3	1.5	pF
CL1	Load capacitance		7		pF

Under such CL range and crystal, the negative resistance (-R) is 3 times more than the crystal series resistance. If larger CL is selected, the frequency accuracy will be decreased, and the negative resistance (–R) will degrade, too.

8.2.4. ESD electrical sensitivity

Table 8.2-9. ESD electrical characteristic of MT2533D

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ESD mode	Description	Pin name	Min.	Max.	Unit
HBM		JESD22-A114-F	-2000	2000	V
CDM	All pins exclude corner pins	JESD22-C101-D	-500	500	V
	Corner pins	JESD22-C101-D	-750	750	V

8.3. Display controller

The display controller provides MIPI DBI TYPE-C (Display Bus Interface — a serial data transfer type interface mode and MIPI DSI (Display Serial Interface) interface mode with the following features:

- Supports four layers of overlay with individual color depth, window size, vertical and horizontal offset, source key, dither and alpha value.
- Supports ARGB8888, PARGB8888, ARGB6666, PARGB6666, RGB888, RGB 565, YUYV422, 1/2/4 index input color formats.
- Supports index color look-up table of up to 16 colors.
- Supports per pixel alpha channel.
- Supports hardware display rotation.
- Supports true color engine.
- Supports 65K color (RGB565), 262K color (RGB666) and 16M color (RGB888) LCM formats.
- Supports adaptive ambient light control for DRE enhancement and CABC compensation for sunlight visibility and backlight power saving.

8.3.1. MIPI DBI TYPE-C interface

MIPI DBI TYPE-C interface has the following features:

- Supports LCD module with maximum resolution of up to 320 x 320 (when operating in 2-data-pin mode).
- Supports 3-wire and 4-wire serial data interface (9/10/16/18-bit data per transaction).
- Supports 2-data-pin serial interface (16/18/24-bit data per transaction).
- Supports `cs_stay_low` and `single A0` mode.
- Supports start byte mode.
- Capable of simultaneous connection to two serial LCD modules (LSCE0, LSCE1).

8.3.2. MIPI DSI interface

The display serial interface (DSI) is based on MIPI Alliance Specification, supporting high-speed serial data transfer between the host processor and peripheral devices, such as display modules. DSI supports command mode data transfer defined in MIPI specifications, and it also provides bidirectional transmission with low-power mode to receive messages from the peripherals.

The DSI engine has the following features:

- One clock lane and one data lane.

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- Throughput of up to 100 Mbps for one data lane.
- Bidirectional data transmission in low-power mode in data lane 0.
- Uni-directional data transmission in high-speed mode in data lane 0.
- DCS command transmission.
- Pixel format of RGB565/loosely RGB666/RGB888.
- Supports non-continuous high-speed transmission in all data lanes.
- Supports peripheral TE and external TE signal detection.
- Supports ultra-low power mode control.

8.4. MIPI DBI TYPE-C interface characteristics

For 3-wire serial data interface:

- LSCE: Chip select, a falling edge of this signal indicates the start of transmission. The interface will be initialized when this signal is HIGH.
- LSCK: Serial transfer clock.
- LSDA: Serial input/output data.

For 4-wire serial data interface:

- LSCE: Chip select, a falling edge of this signal indicates the start of transmission. The interface will be initialized when this signal is HIGH.
- LSCK: Serial transfer clock.
- LSDA: Serial input/output data.
- LSA0: Data/command select. Will be HIGH if there is data transaction; otherwise LOW.

For 2-data-pin mode:

- LSCE: Chip select, a falling edge of this signal indicates the start of transmission. The interface will be initialized when this signal is HIGH.
- LSCK: Serial transfer clock.
- LSDA: Serial input/output data.
- LSA0: Serial output data.

8.4.1. Serial data write mode

Figure 8.4-1, Figure 8.4-2 and Figure 8.4-3 show the timing diagram of write operation for different interfaces. The interface characteristics are listed in Table 8.4-1.

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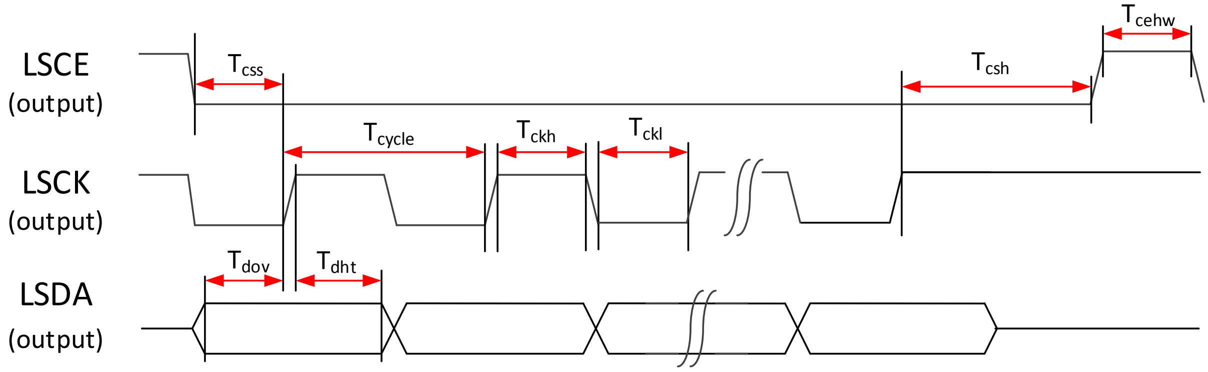

Figure 8.4-1. 3-wire serial data interface

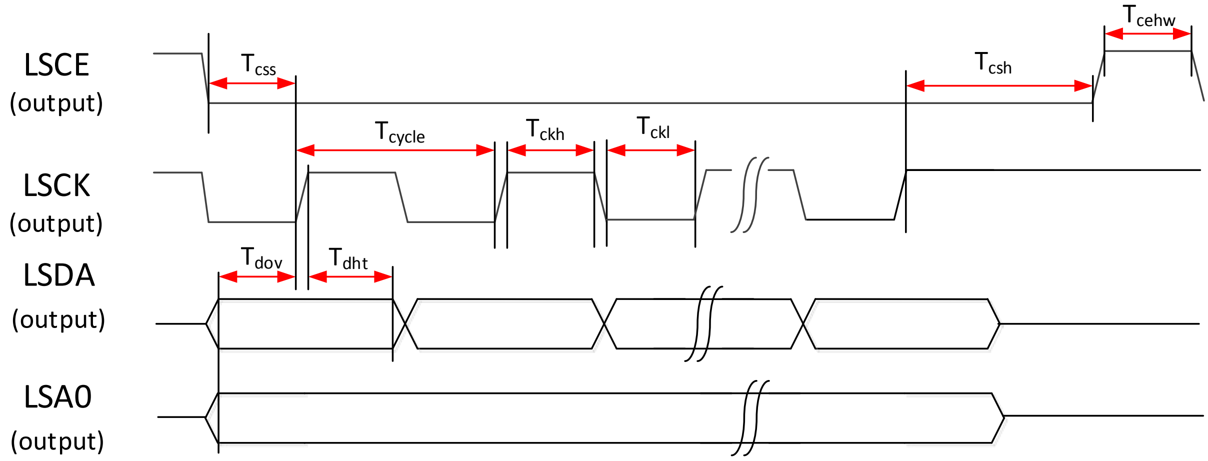

Figure 8.4-2. 4-wire serial data interface

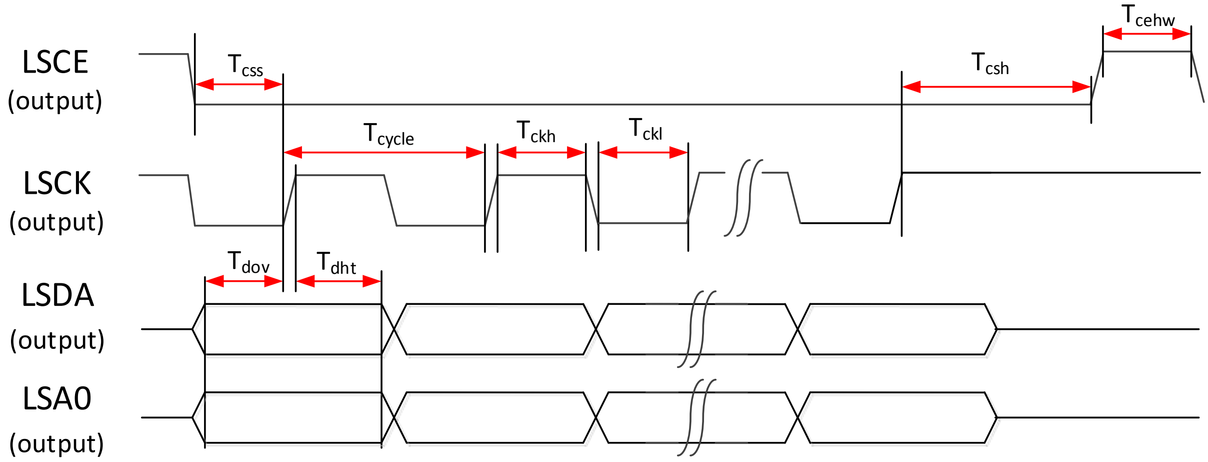

Figure 8.4-3. 2-data pin mode

Table 8.4-1. Serial interface characteristics during write operation

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
LSCK	Tcycle	Serial clock cycle	16	-	ns	
	Tckh	Clock High pulse width	7.2	-	ns	

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Signal	Symbol	Parameter	Min.	Max.	Unit	Description
	Tckl	Clock Low pulse width	7.2	-	ns	
LSCE	Tcehw	Chip select High pulse width	16	-	ns	
	Tcss	Chip select valid time	15	-	ns	
	Tcsh	Chip select hold time	15	-	ns	
LSDA/LSA0	Tdov	Data output valid time	7	-	ns	
	Tdht	Data output hold time	7	-	ns	

8.4.2. Serial Data Read Mode

Figure 8.4-4. shows the timing diagram of read operation. The interface characteristics are listed in Table 8.4-2.

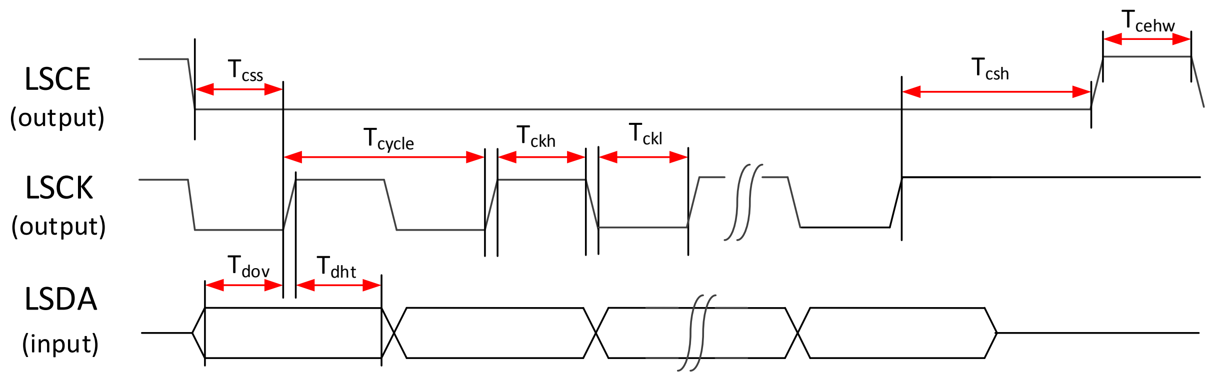

Figure 8.4-4. 3-wire serial interface

Table 8.4-2. Serial interface characteristics during read operation

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
LSCK	Trcycle	Serial clock cycle (read)	67	-	ns	
	Trckh	Read clock High pulse width (read)	33	-	ns	
	Trckl	Clock Low pulse width (read)	33	-	ns	
LSCE	Trcehw	Chip select High pulse width (read)	67	-	ns	
	Trcss	Chip select valid time (read)	44	-	ns	
	Trcsh	Chip select hold time (read)	44	-	ns	
LSDA/LSA0	Tridrs	Input data required setup time (read)	33	-	ns	
	Tridrh	Input data required hold time (read)	33	-	ns	

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8.5. MIPI DBI TYPE-C Interface Color Coding

8.5.1. 3-wire Serial Data Interface Write (A0+8-bit)

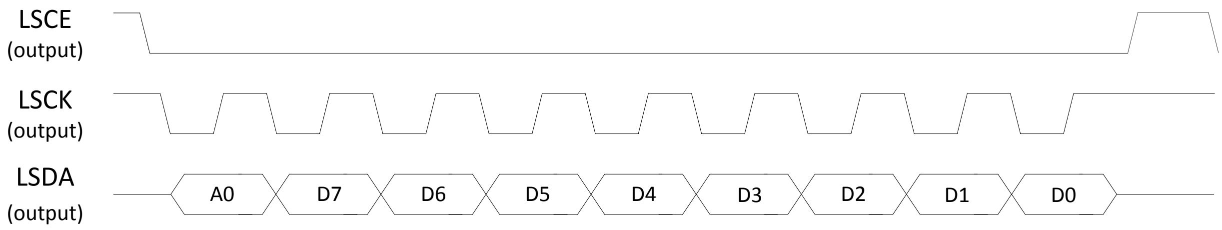

Figure 8.5-1. 3-wire serial interface (A0+8-bit)

- For RGB565 output format:

D[15:0] = { R[4:0], G[5:0], B[4:0] }, 1 pixel/2 transactions

- For RGB666 output format:

{ D[23:18], D[15:10], D[7:2] } = { R[5:0], G[5:0], B[5:0] }, 1 pixel/3 transactions

- For RGB888 output format:

D[23:0] = { R[7:0], G[7:0], B[7:0] }, 1 pixel/3 transactions

8.5.2. 3-wire Serial Data Interface Write (A0+9-bit)

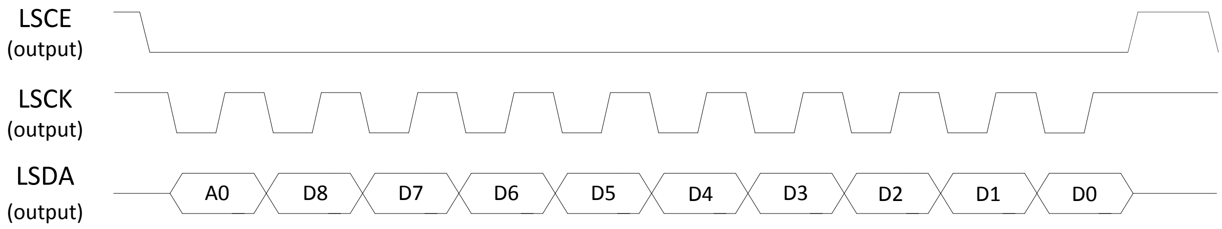

Figure 8.5-2. 3-wire serial interface (A0+9-bit)

- For RGB666: D[17:0] = { R[5:0], G[5:0], B[5:0] }, 1 pixel/2 transactions

Three other modes:

1) A0+ 16-bit mode for RGB565: 1 pixel/1 transaction
2) A0+ 18-bit mode for RGB666: 1 pixel/1 transaction
3) A0+ 24-bit mode for RGB888: 1 pixel/1 transaction

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8.5.3. 4-wire Serial Data Interface Write (8-bit)

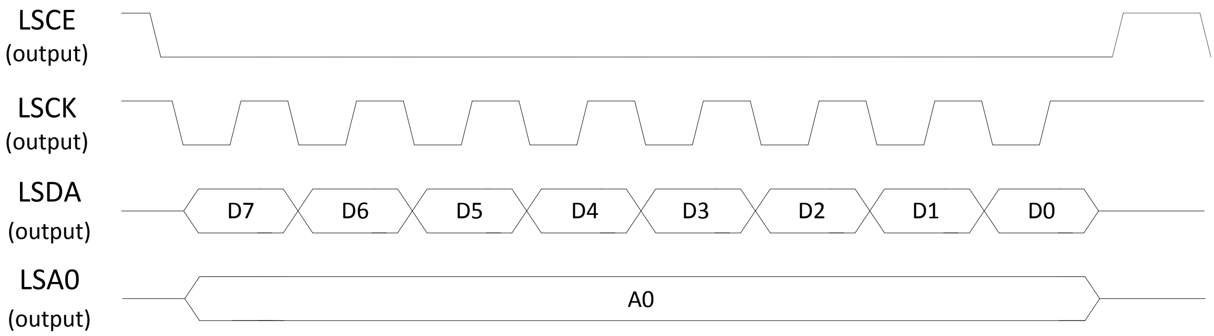

Figure 8.5-3. 4-wire serial interface write (8-bit)

- For RGB565:

D[15:0] = { R[4:0], G[5:0], B[4:0] }, 1 pixel/2 transactions

- For RGB666:

{ D[23:18], D[15:10], D[7:2] } = { R[5:0], G[5:0], B[5:0] }, 1 pixel/3 transactions

- For RGB888:

D[23:0] = { R[7:0], G[7:0], B[7:0] }, 1 pixel/3 transactions

Four other modes:

1) 9-bit mode for RGB666: 1 pixel/2 transactions
2) 16-bit mode for RGB565: 1 pixel/1 transaction
3) 18-bit mode for RGB666: 1 pixel/1 transaction
4) 24-bit mode for RGB888: 1 pixel/1 transaction

8.5.4. 2-data-pin Mode Write (A0+8-bit)

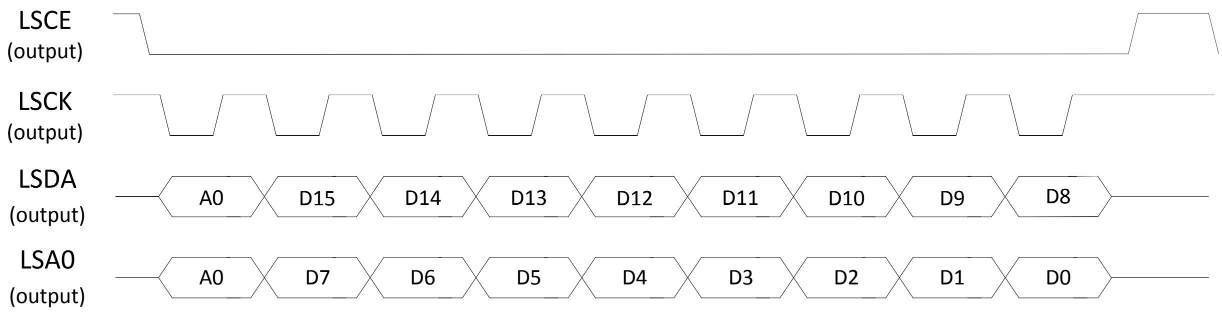

Figure 8.5-4. 2-data-pin mode write (A0+8-bit)

- For RGB565:

D[15:0] = { R[4:0], G[5:0], B[5:0] }, 1 pixel/1 transaction

- For RGB888:

D[47:23] = { R1[7:0], G1[7:0], B1[7:0] }

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D [23: 0] = { R0[7:0], G0[7:0], B0[7:0] }, 2 pixels/3 transactions

8.5.5. 2-data-pin Mode Write (A0+9-bit)

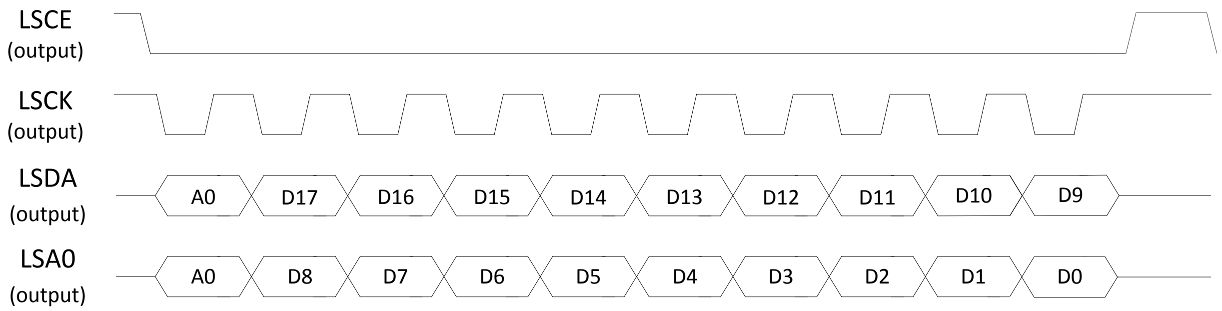

Figure 8.5-5. 2-data-pin mode write (A0+9-bit)

- For RGB666:

D[17:0] = { R[5:0], G[5:0], B[5:0]}, 1 pixel/1 transaction

8.5.6. 2-data pin Mode Write (A0+12-bit)

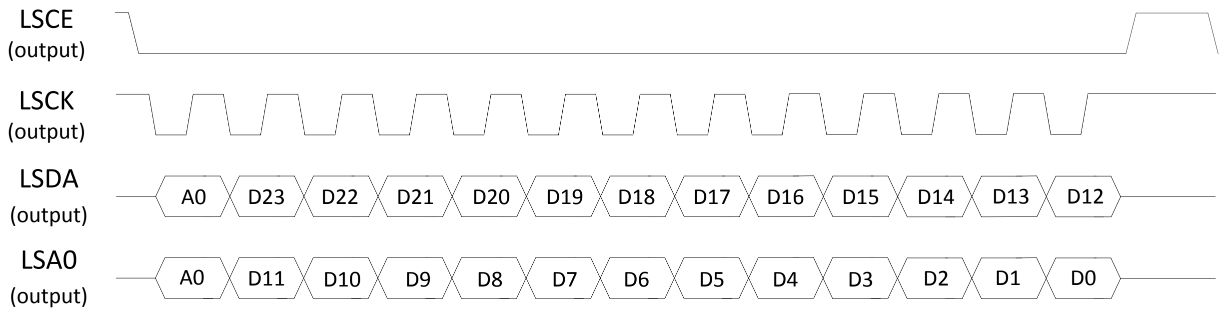

Figure 8.5-6. 2-data-pin mode write (A0+12-bit)

- For RGB888:

D[23:0] = { R{7:0], G[7:0],B [7:0] }, 1 pixel/1 transaction

8.6. MIPI DSI interface characteristics

8.6.1. HS clock transmission

Figure 8.6-1 shows high-speed clock transmission waveform. The parameters on the figure are listed in Table 8.6-1.

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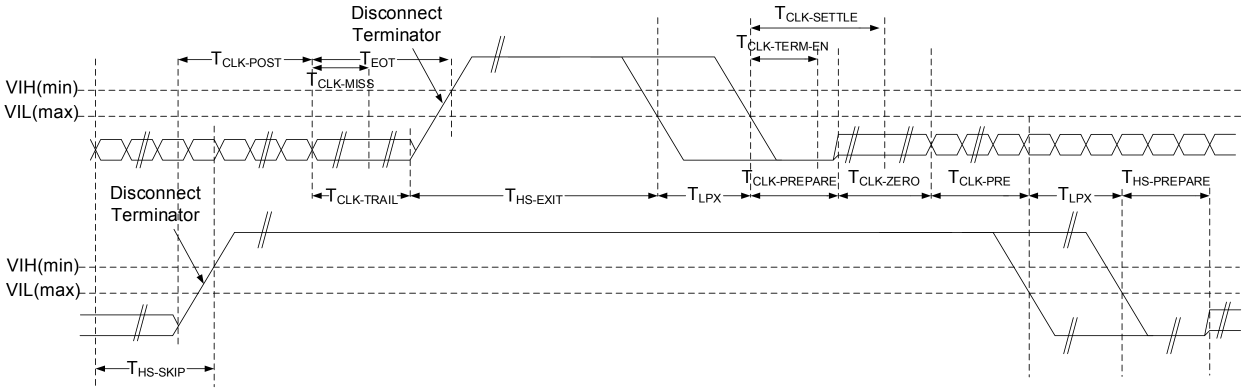

Figure 8.6-1. HS clock transmission

Table 8.6-1. HS clock transmission timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
TCLK-MISS	Timeout for receiver to detect absence of clock transitions and disable the Clock Lane HS-RX			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP mode. The interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI			ns
TCLK-PRE	Time that the HS clock should be driven by the transmitter prior to any associated Data Lane starting the transition from LP to HS mode	8			ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starts the HS transmission	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver should ignore any Clock Lane HS transition, starting from the beginning of TCLK-PREPARE	95		300.0	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX	Time for Dn to reach VTERM-EN		38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the clock	300			ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst			105 ns + n*12*UI	ns

8.6.2. HS data transmission

Figure 8.6-2 shows high-speed clock transmission waveform. The parameters on the figure are listed in Table 8.6-2.

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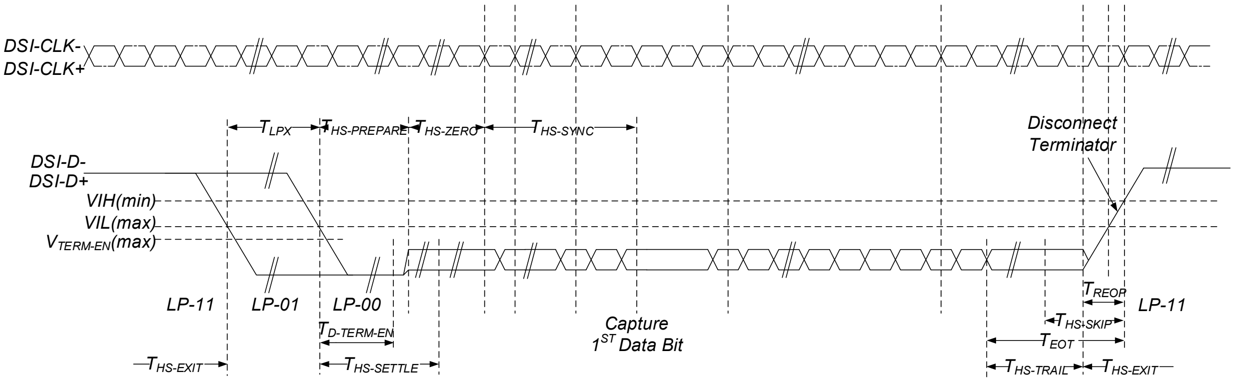

Figure 8.6-2. HS data transmission in bursts

Table 8.6-2. HS data transmission timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL, MAX	Time for Dn to reach VTERM-EN		35 ns + 4*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst	100			ns
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starts the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the sync sequence	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver should ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE. The HS receiver should ignore any Data Lane transition before the minimum value, and the HS receiver should respond to any Data Lane transition after the maximum value.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)			ns

8.6.3. Turnaround procedure

Figure 8.6-3 and Figure 8.6-4 show the turnaround procedure. The parameters on the figure are listed in Table 8.6-3.

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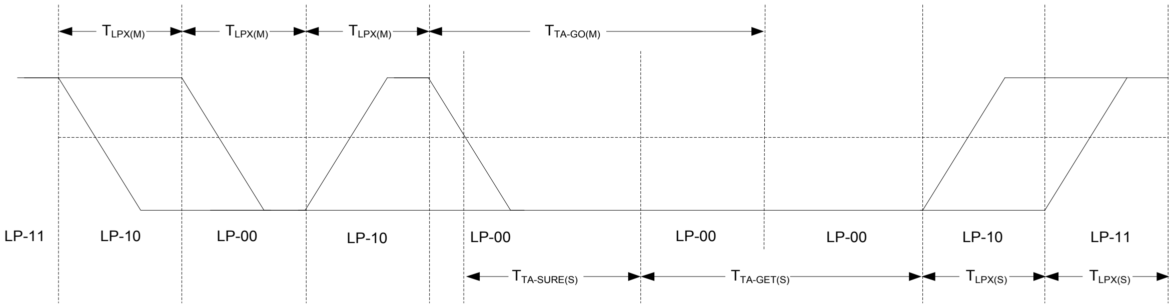

Figure 8.6-3. Turnaround procedure from MCU to display module

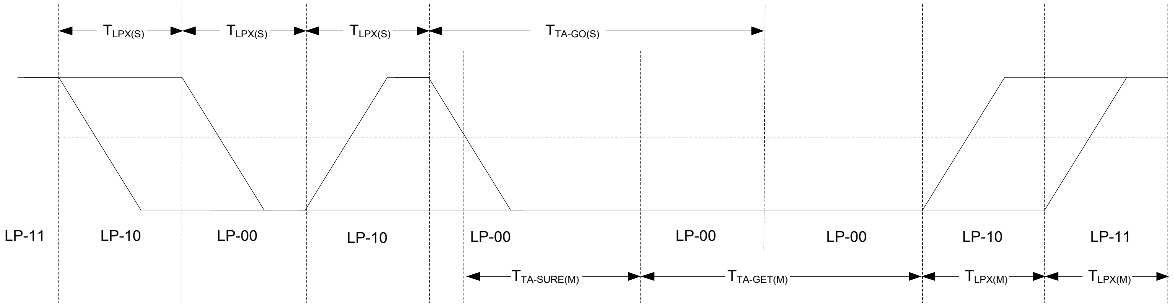

Figure 8.6-4. Turnaround procedure from display module to MCU

Table 8.6-3. Low power mode timing parameter

Parameter	Description	Min.	Typ.	Max.	Unit
TLPX(M)	Transmitted length of any Low-Power state period from MCU to display module	100			ns
TTA-GET(M)	Time that the MCU drives the Bridge state (LP-00) after accepting control during a Link Turnaround		5*TLPX		ns
TTA-GO(M)	Time that the MCU drives the Bridge state (LP-00) before releasing control during a Link Turnaround		4*TLPX		Ns
TTA-SURE(M)	Time that the MCU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround	TLPX		2*TLPX	Ns
TLPX(D)	Transmitted length of any Low-Power state period from display module to MCU	100			Ns
TTA-GET(D)	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		Ns
TTA-GO(D)	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround		4*TLPX		Ns
TTA-SURE(D)	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround	TLPX		2*TLPX	Ns

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8.7. MIPI DSI interface color coding

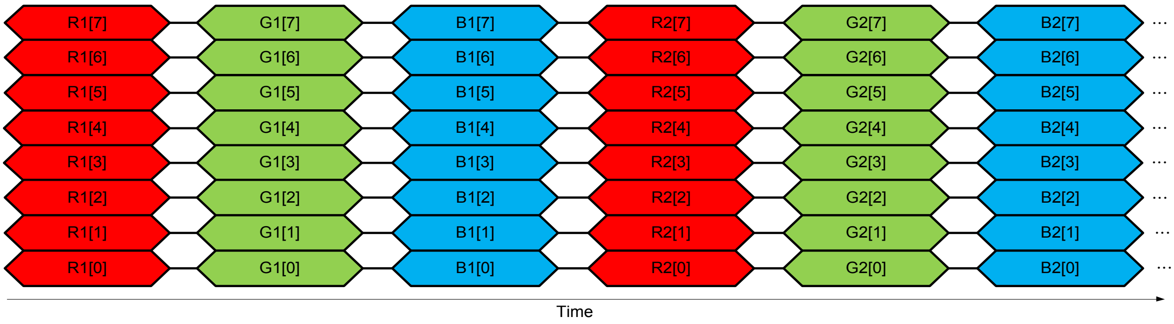

Figure 8.7-1. Pixel format of RGB565

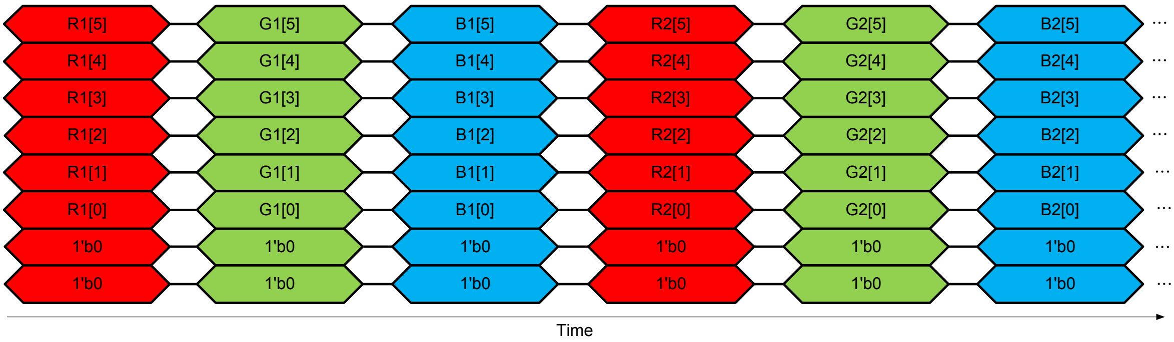

Figure 8.7-2. Pixel format of loose RGB666

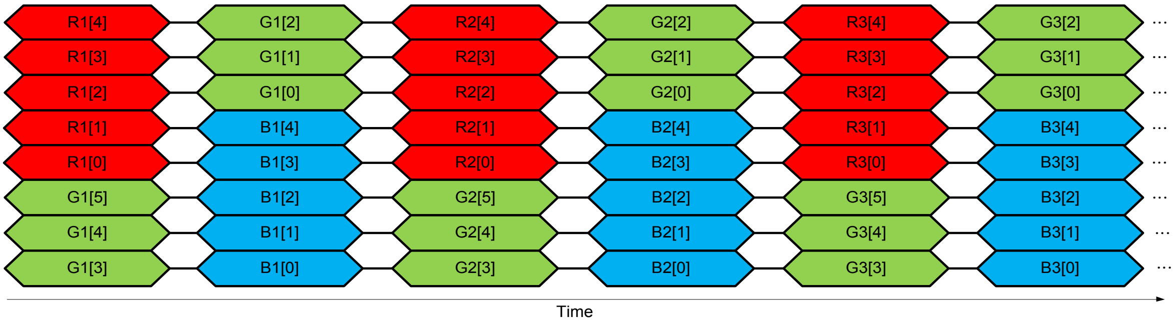

Figure 8.7-3. Pixel format of RGB565

8.8. Power On/Off sequence

Power on/off sequence (VCORE, VIO18, PIO_VCORE_PREON, PIO_RESETB, VIO28, AVDD33_USB can be powered off simultaneously):

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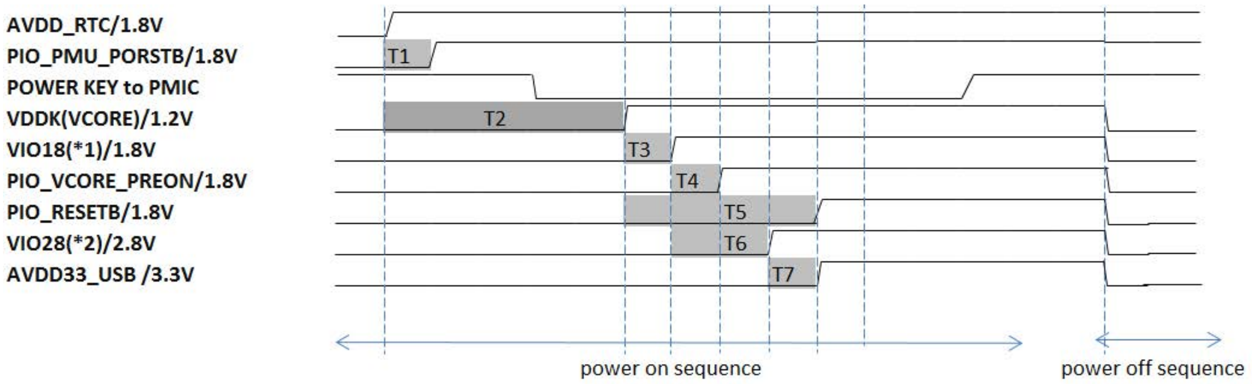

T1 >= 1ms: PIO_PMU_PORSTB delay at least 1ms to AVDD_RTC
T2 >= 100ms: VCORE delay at least 100ms to AVDD_RTC
T3 >= 0ms: VIO18 not earlier than VCORE
T4 >= 1ms: PIO_VCORE_PREON at least 1ms to VIO18
T5 >= 25ms: PIO_RESETB delay at least 25ms to VCORE
T6 >= 3ms: VIO28 delay at least 3ms to VIO18
PIO_RESETB released at least 3ms later than VIO28
T7 >= 0ms: AVDD33_USB not earlier than VIO28
After PIO_RESETB released, AVDD33_USB need power up within 100ms

(*1) VIO18 = VIO18, AVDD18_DCXO
(*2) VIO28 = AVDD28_ABB, DVDD_AUXADC

Figure 8.8-1. Power on/off sequence

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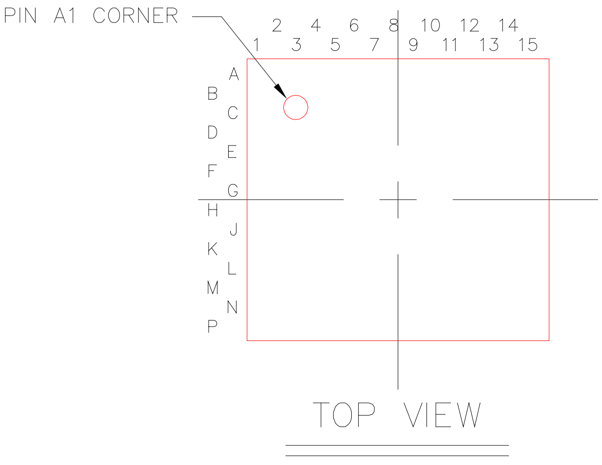
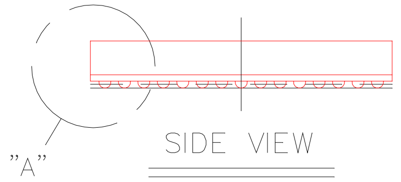
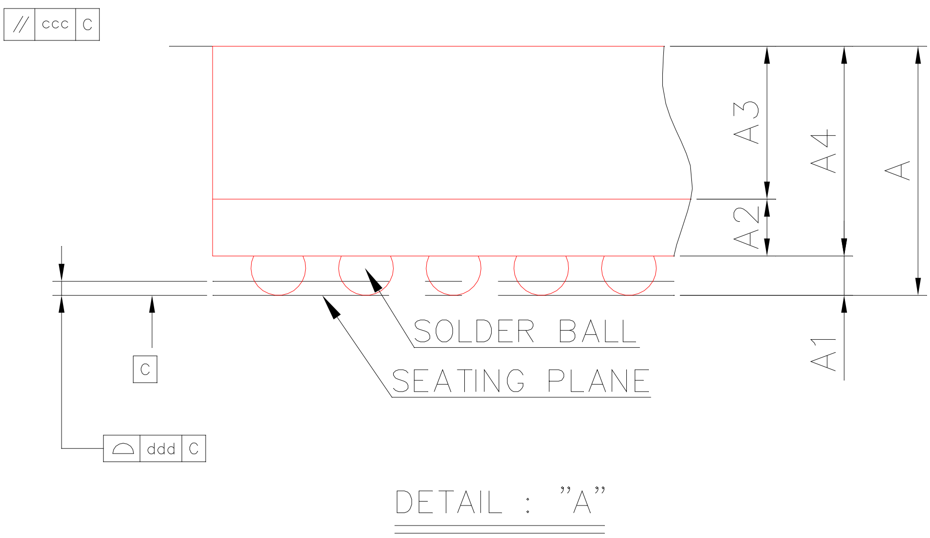
9. Package Information

9.1. MT2533D mechanical data of the package







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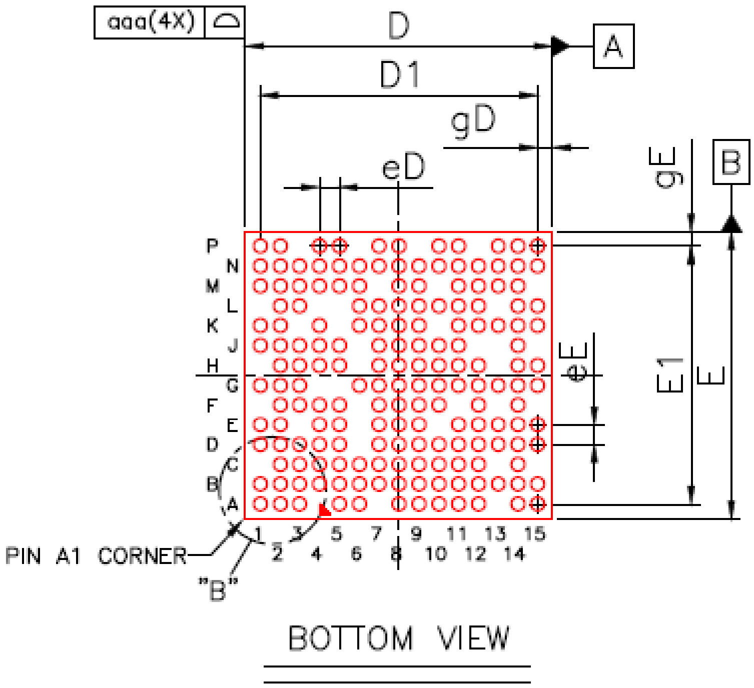

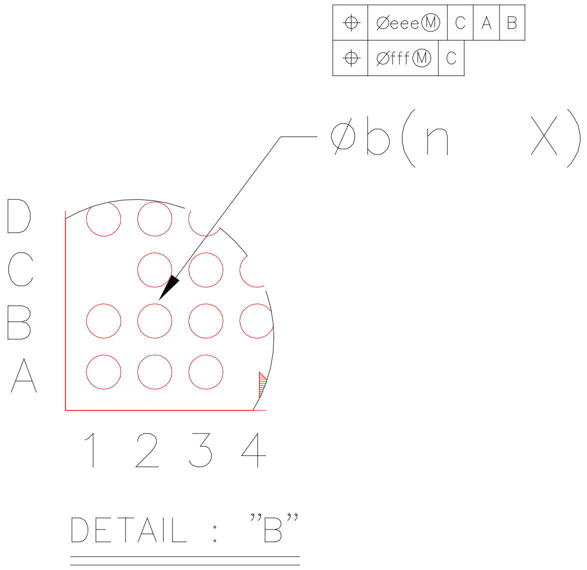

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Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				TFBGA	
Body Size	X	D	6.10	6.20	6.30
	Y	E	5.70	5.80	5.90
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.70 Ref.	
Substrate Thickness		A2		0.13 Ref.	
Substrate+Mold Thickness		A4	0.78	0.83	0.88
Total Thickness		A	–	–	1.05
Ball Diameter				0.25	
Ball Stand Off		A1	0.10	0.15	0.20
Ball Width		b	0.22	0.27	0.32
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		172	
Edge Ball Center to Center	X	D1		5.60	
	Y	E1		5.20	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

Figure 9.1-1 Outlines and dimensions of MT2533D TFBGA 6.2 mm*5.8 mm, 165-ball, 0.4 mm pitch package

9.2. MT2533D thermal operating specifications

Table 9.2-1. MT2533D thermal operating specifications

Description	Value	Unit
Thermal resistance from device junction to package case	14.23	C/W
Maximum package temperature	65	Deg C
Maximum power dissipation	0.55	W

9.3. MT2533D lead-free packaging

The MT2533D platform is provided in a lead-free package and meets RoHS requirements.

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10. Ordering Information

10.1. MT2533D top marking definition

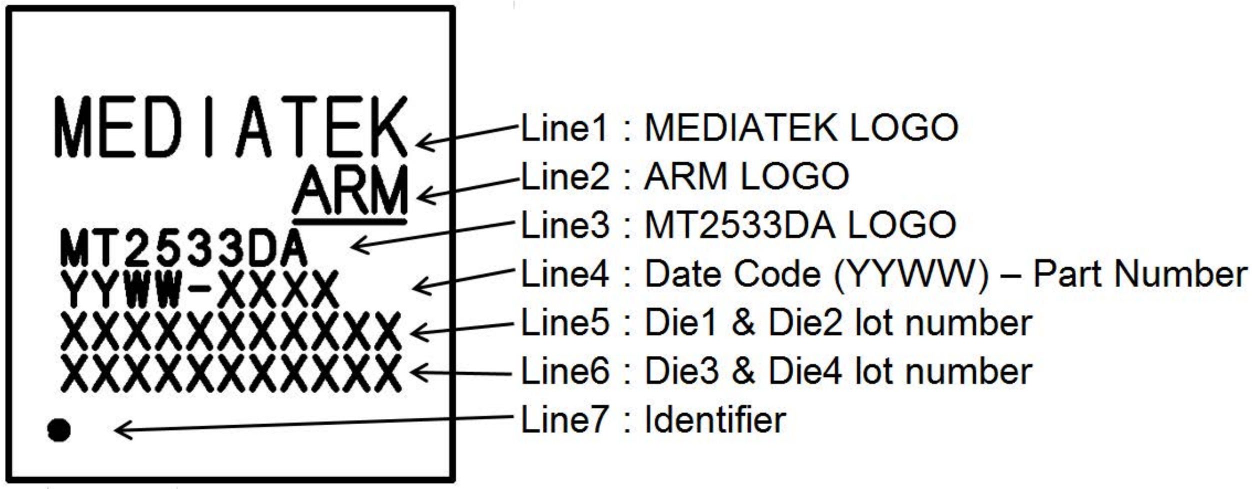

Figure 10.1-1. Mass production top marking of MT2533D

Table 10.1-1. Ordering information

Product number	Package	Description
MT2533DA/A	TFBGA	6.2mm*5.8mm, 172-ball, 0.4mm pitch Package, non-security version

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